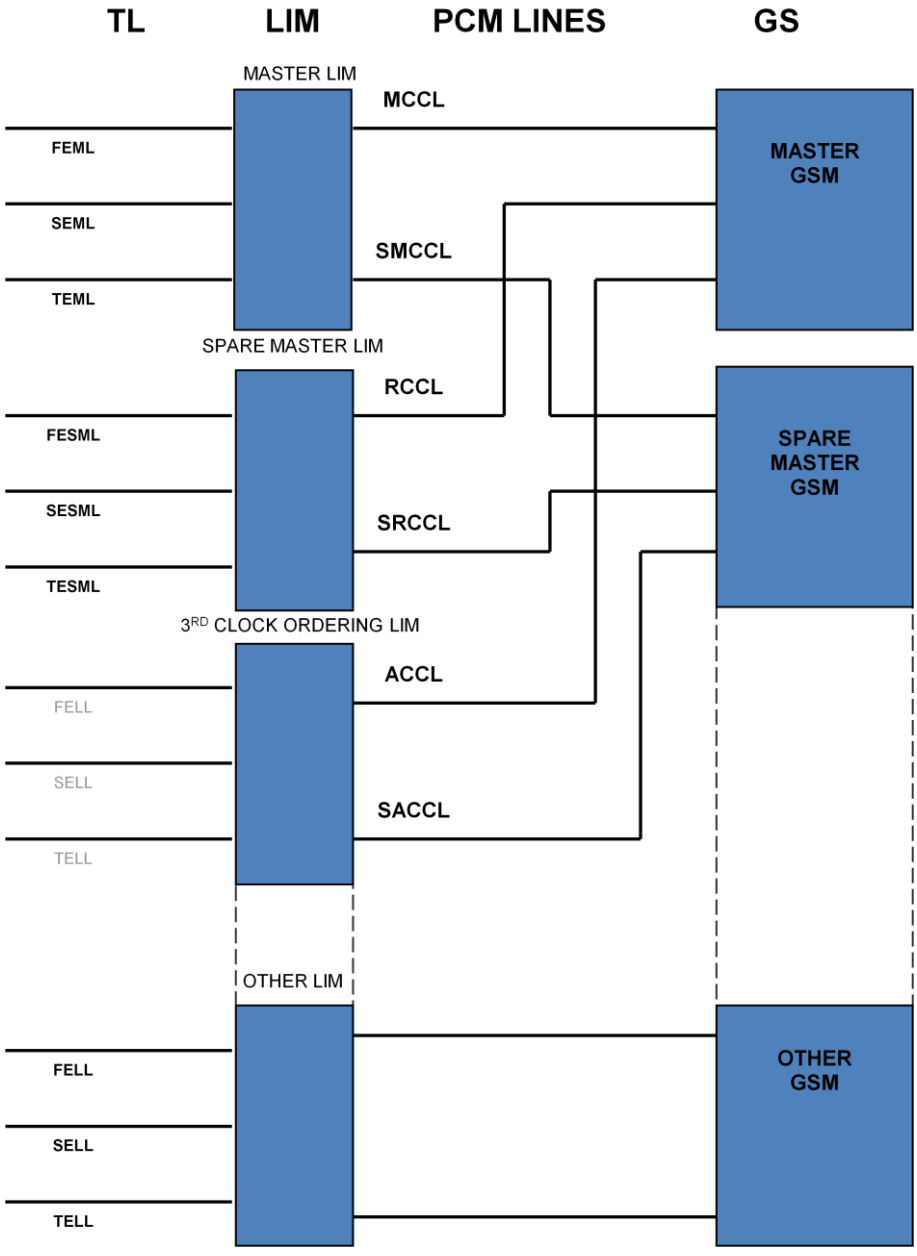
MX-One Synchronisation with a Group Switch

GENERAL

This document contains a brief comparison between the synchronisation methods of MX-One TSE with Group Switch and the MD110. Assumption is made that the synchronisation strategy and nomenclature of the MD110 is already understood.

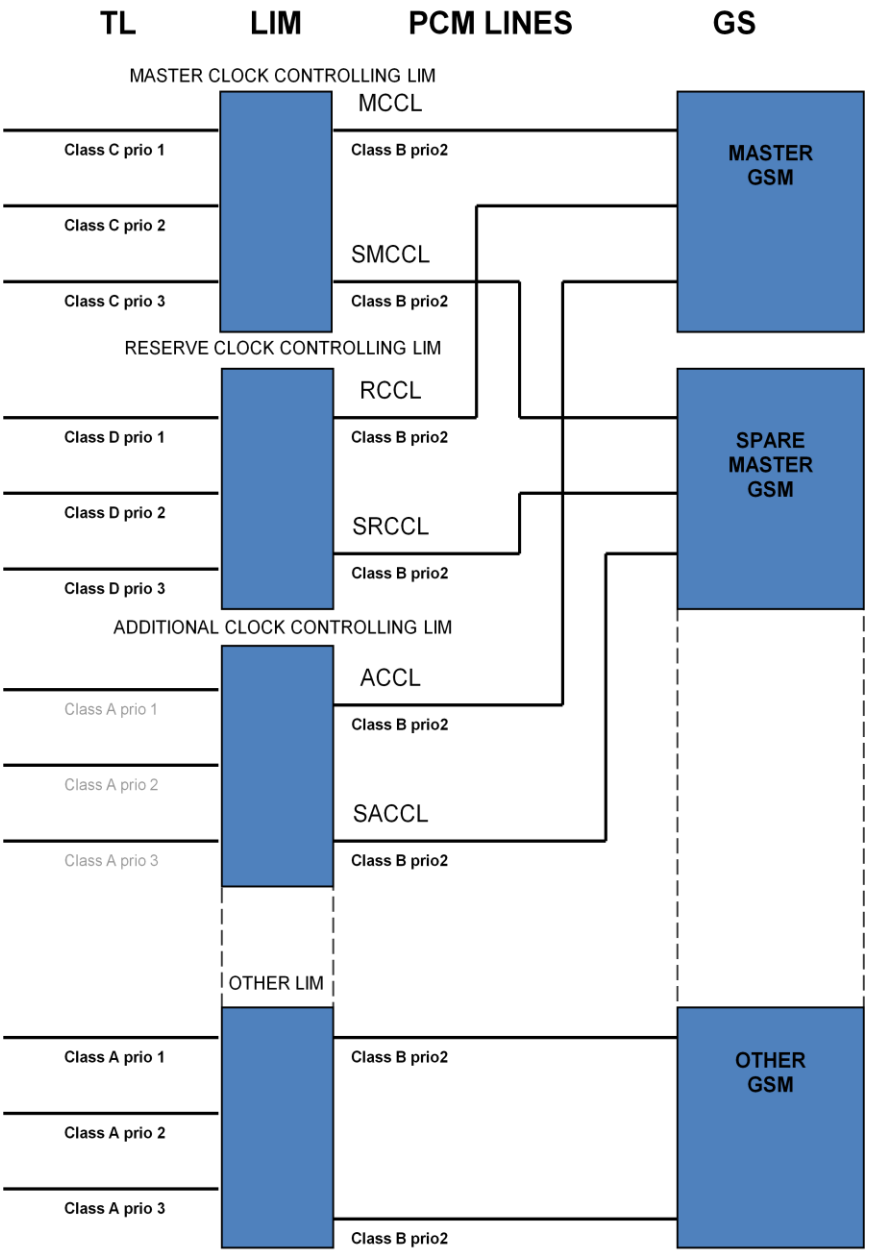
References to the names of the clock ordering LIMs vary across the official documentation especially the designation of the third LIM. Designations used here are taken from the BC12 Function Specification for Synchronization. Just to confuse things further, the designations of the three clock-ordering LIMs have been changed for MX-One.

MD110 CONFIGURATION




```
SCICI:MCCL RCCL ACCL SMCCL SRCCL SACCL
SCEXI:FEML SEML TEML FESML SESML TESML    <- Master LIM and SpareMaster LIM
SCEXI:FELL SELL TELL                      <- Other LIMs
```

MX-ONE CONFIGURATION



pcm_synchronization –mlim –rlim –alim
trsp_synchronization –class –prio –bpos

Synchronisation values in **trsp_synchronization** (TRASER) are compared between Master and Reserve LIMs, so that the best Class with highest Priority will determine which LIM will provide synchronisation to the Group Switch.

In the example above, all three external sources in the Master LIM will take precedence over the external sources in the Reserve LIM.

Making the PCM links ‘Class B Priority 2’ ensures that the LIM which is not supplying synchronisation to the Group Switch will receive synchronisation from it. The exception being those LIMs with external synchronisation set to a higher class/priority than the PCM link, these LIMs will always synchronise to their own available external sources.