ORDER NO. KMS9703201C1

F.5

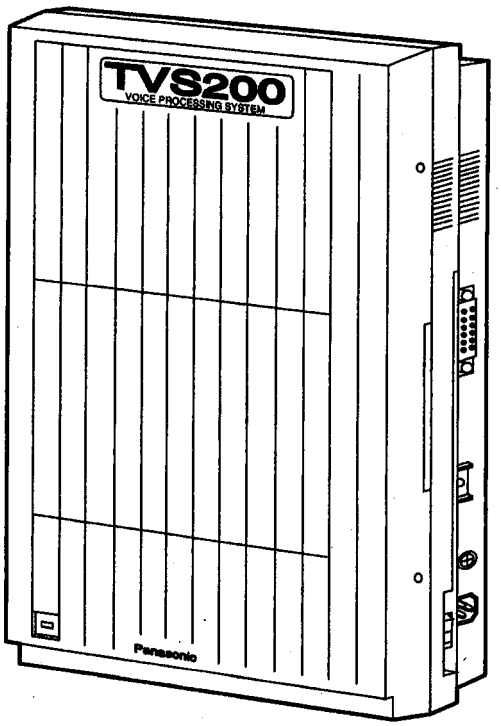
Service Manual

VOICE PROCESSING SYSTEM

KX-TVS200

(KX-TVS204)

For U. S. A.



⚠ WARNING

This service information is designed for experienced repair technicians only and is not designed for use by the general public.
It does not contain warnings or cautions to advise non-technical individuals of potential dangers in attempting to service a product.
Products powered by electricity should be serviced or repaired only by experienced professional technicians.
Any attempt to service or repair the product or products dealt with in this service information by anyone else could result in serious injury or death.

Panasonic

When referring to the serial number, supply all 11 digits. The serial number may be found on the label affixed to the back of the unit.

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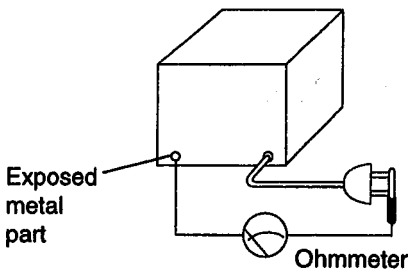
SAFETY PRECAUTIONS

1. Before servicing, unplug the power cord to prevent an electric shock.
2. When replacing parts, use only the manufacturer's recommended components for safety.
3. Check the condition of the power cord. Replace if wear or damage is evident.
4. After servicing, be sure to restore the lead dress, insulation barriers, insulation papers, shields, etc.
5. Before returning the serviced equipment to the customer, be sure to perform the following insulation resistance test to prevent the customer from being exposed to shock hazards.

INSULATION RESISTANCE TEST

1. Unplug the power cord and short the two prongs of the plug with a jumper wire.
2. Turn on the power switch.
3. Measure the resistance value with ohmmeter between the jumpered AC plug and each exposed metal cabinet part, such as screwheads, control shafts, handle brackets, etc.
   ***Note:** Some exposed parts may be isolated from the chassis by design. These will read infinity.
4. If the measurement is outside the specified limits, there is a possibility of shock hazard. The equipment should be repaired and rechecked before it is returned to the customer.



Resistance = more than 1 MΩ (at DC 500 V)

FOR SERVICE TECHNICIANS

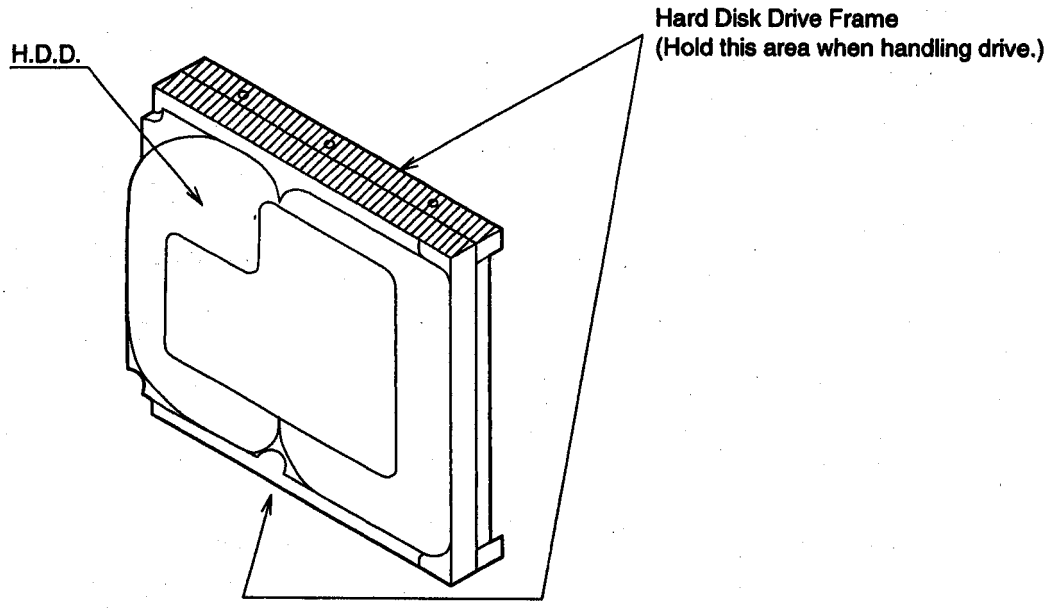
ICs and LSIs are vulnerable to static electricity.
When repairing, the following precautions will help prevent recurring malfunctions.
1) Cover the plastic parts boxes with aluminum foil.
2) Ground the soldering irons.
3) Use a conductive mat on the worktable.
4) Do not touch IC or LSI pins with bare fingers.

Take special care when handling the Hard Disk Drive unit and KX-TVS200.

WARNING

CAUTION When Handling Hard Disk Drive!

1) Beware of static electricity when handling the hard disk drive.
2) Do not touch circuit area.
3) Avoid hitting the drive with screwdriver when tightening screws.
4) Do not insert connector or tighten screws while pressing down on the surface of the hard disk drive. (Hold the hard disk drive frame when inserting connector or tightening screws.)
5) The hard disk drive is extremely sensitive to impact; handle with care. Do not drop or jar.



CAUTION

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to following caution:

Disposal of lithium batteries should be performed by permitted, professional disposal firms knowledgeable in state government federal and local hazardous materials and hazardous waste transportation and disposal requirements.
Battery continues to have no transportation limitations as long as they are separated to prevent short circuits and packed in strong packaging.
Commercial firms that dispose of any quantity of lithium cells should have a mechanism in place to account for their ultimate disposition. This is a good practice for all types of commercial or industrial waste.

Recommend Type Number: CR23541(BATT) Manufactured by MATSUSHITA

SPECIFICATIONS

Ports :		2 to 8 DPITS interface, or 2 to 6 SLT interface
Dialing Method :		Tone duration/Pulse (10/20pps)*
Flash time :		100/300/600/900 msec (programmable)*
CPC Detection :		None/6.5/150/300/450/600 msec (programmable)*
Extension numbering :		2 to 5 digits (programmable)
Pause time :		1 to 9 sec (programmable)
Main CPU :		16 bit microprocessor
Capacity for Hard Disk :		32 hours
Number of Mailboxes :		Max. 1024
Number of Messages :		Max. 100 per mailbox (programmable)
Maximum Message Length :		1 to 6 min. (programmable)
Message Retention Time :		1 to 30, or unlimited (programmable)
Reports :		Mailbox List, Class of Service List, System Service Report, Call Account Report, Port Usage Report, Mailbox Usage Report, FAX Report
Connections	Telephone line :	Modular connectors 2-conductor wire with SLT interface 4-conductor wire with DPITS interface
	Data port :	RS-232C interface port
Power Source :		AC 120V, 60 Hz
Dimensions (H × W × D):		468 × 327 × 101 mm (18-7/10" × 12-7/8" × 4")
Weight:		5.3 Kg (11 lb 11 oz)

*Using with SLT interface card

OVER VIEW

This chapter describes the hardware overview of the Voice Processing System (VPS).

1. SYSTEM OUTLINE

The Panasonic Voice Processing System (VPS) is a voice prompted, menu-driven system which provides fully automated call transfer (to an extension or mailbox), and voice message receiving and delivery service. Even firsttime users can easily reach their desired extension or mailbox by following step-by-step voice instructions. The VPS works with a PBX as an extension. It can be expanded to handle up to eight simultaneous calls and store up to 32 hours of voice data.

The VPS attends to incoming calls, then transfers those calls to the respective extensions. When owners of extensions cannot answer the call, the mailboxes in the system take messages for them. Owners of the mailboxes can record personal greeting messages with their own voice for callers who enter the mailbox to leave messages.

The VPS has up to 1022 personal mailboxes for subscribers and two special function mailboxes for the System Manager and Message Manager.

The VPS can be used by any caller, and by subscribers (Mailbox Owner) in your company.

Even if the user is away from the office, VPS can be used with any touch tone telephone.

Even callers using a rotary telephone can leave messages or be connected with the operator.

The VPS provides the following incoming call services to callers.

1-1. Automated Attendant (A.A.) Service

The automated Attendant works as a receptionist would by answering incoming calls without human intervention.

The Automated Attendant plays a list of options (calling extension, calling operator, Department Dialing, Dialling by Name) to a caller with a voice prompt. When an option has been selected, the Automated Attendant responds to the command by either routing the caller to an extension or the operator. The Automated Attendant will even respond if the extension is busy or if there is no answer.

One option is to let the caller leave a message in a mail box.

1-2. Voice Mail (V.M.) Service

Voice Mail is a voice message receiving and delivery service which allows subscribers (the owner of a personal mailbox) to receive messages in their mail box whether they are out of the office, on the line, or just unavailable to answer the call.

Any caller can leave a message in a subscriber's mailbox. The subscriber can listen, transfer, and deliver recorded messages at any time from anywhere in the world.

1-3. Interview Service

You can set up a questionnaire mailbox with as many as 10 questions, and obtain specific information from customers calling into the system. Between each recorded question, the VPS collects a reply from the caller and stores it in a mailbox.

This service is ideal for gathering any data from product orders to requests for repairs.

1-4 Custom Service

The Custom Service capability optimizes the application of the VPS to meet your business needs. Your callers can access the services or people they need by pressing a single digit on their telephone keypad.

As many as two custom service scripts can be assigned to each VPS port (Day Service and Night Service).

2. SYSTEM PROGRAMMING

This system can be programmed either by a data terminal (VT100, compatibles, or other ASCII terminals) through the System Administrator Interface or by telephone (touch tone telephone) through the System Manager mailbox.

2-1. Terminal Based Programming

After system installation, it is recommended that you perform "Quick Setup" first.

<Quick Setup>

Provides a fast way of setting up the VPS for basic Voice Mail or Automated Attendant service. This includes mailbox creation, incoming call service assignment for all ports, time setting and several other programming items which must be done initially to start the VPS operation.

<PBX Integration>

In its initial state, the KX-TVS200 is not provided with an integration port. Integration is enabled by mounting the KX-TVS102 or KX-TVS204 optional card. Typically, each VPS port is connected to an extension port of the PBX.
Between PBX's, the VPS exchanges a request to a counterparty or status for itself mutually, then offers a quick and useful service. The VPS works well with all Panasonic KX-T series PBX's and can be programmed to work with most other manufacturer's PBX's that fully support single line telephone interfaces.
However, because the VPS operation depends on the capabilities and features provided by the PBX, its performance will vary when connected to different PBX's. In system program, Integration Parameter with a PBX should be installed to achieve quicker and more useful service.

2-2. Telephone Based Programming

During daily operation, the person specified as the System Manager can create and/or delete mailboxes, and change Class of Service parameters.

3. SYSTEM CONFIGURATIONS

The most common configuration of the VPS is behind a PBX. The VPS ports are connected to PBX extension ports.

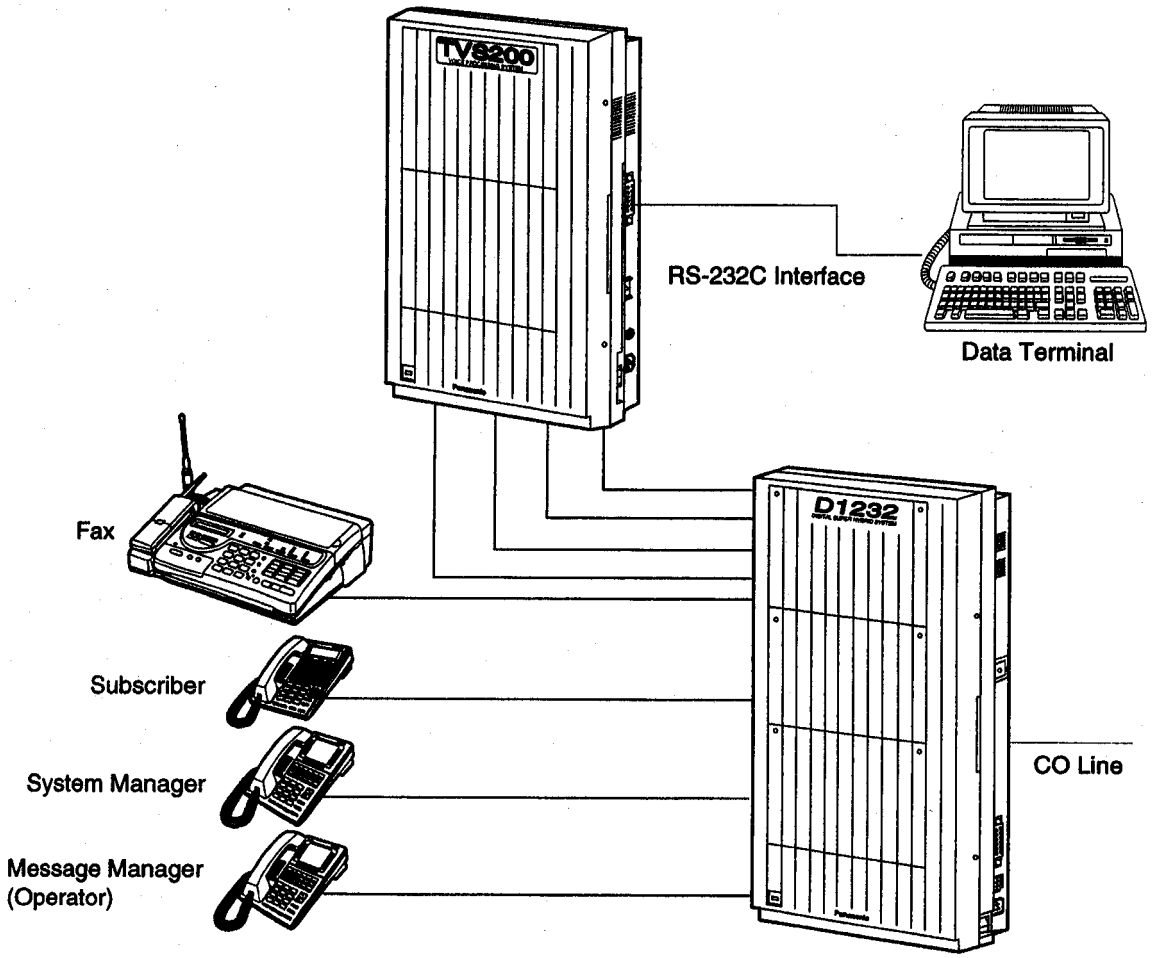


Fig. 1-1. Typical Configurations

4. SYSTEM COMPONENTS

4-1. Outside Equipment

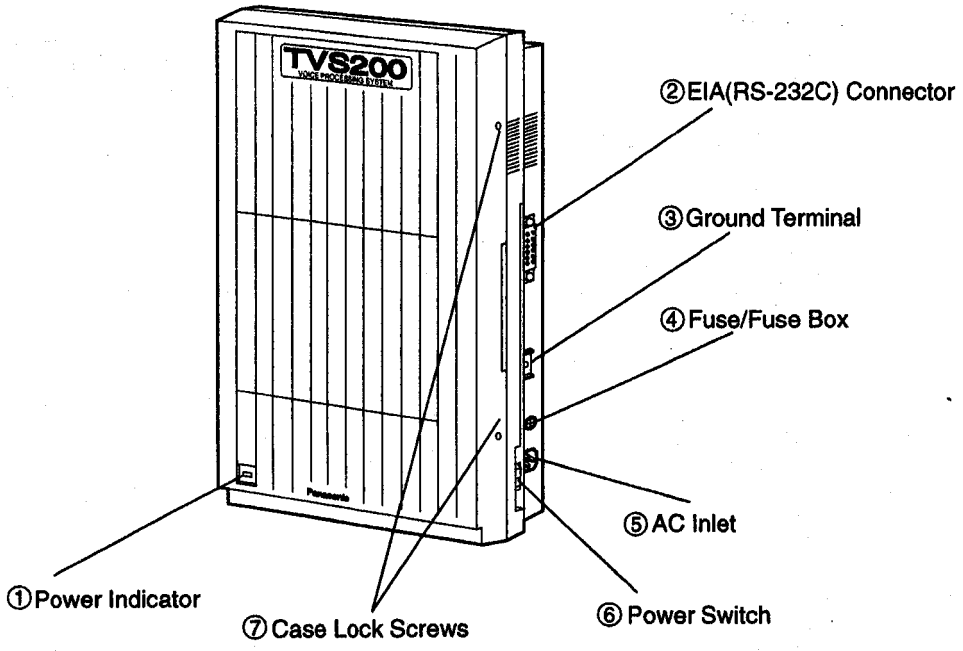


Fig. 1-2. Cabinet Outside View and Equipment Location

①Power Indicator

Power Indicator indicates VPS status. When you turn on the power switch, the power indicator turns on. During this period, the VPS exexutes self diagnostics. When the self diagnostics finishes normally, this indicator starts the blinking sequence. During this period, the VPS executes the system initialization. When this initialization finishes normally, the indicator lights on again, and the VPS stsrts the incoming service. When the VPS detects any error on system, the Indicator informs the type of error by using a specific blinking sequnce.

②EIA (RS-232C) Connector

The VPS allows to communicate with a Data Terminal or with any standard ASCII Terminal for system programming. The terminal is connected to the VPS using an RS-232C cross cable. Attach the 25-pin connector to the jack marked "RS-232C" on VPS.

③Ground Terminal

Ground Terminal is an earth terminal.
Tie the ground line to the Ground Terminal marked "GROUND" on the VPS.

④Fuse/Fuse Box

This fuse is a safety part for AC power line. In order to use the VPS safely, it is required to use a regulated fuse indicated on the label.

⑤AC Inlet

AC inlet is an input connector of AC power source. Attach AC power code to AC Inlet marked "AC IN" on the VPS.

⑥Power Switch

Turn the power switch on the side of marked "ON", then AC Power is supplied to the VPS.
Turn the power switch on the side of marked "OFF", then supply of AC Power is cut.

⑦Case Lock Screws

The VPS has two case lock screws to open the front cover.

4-2. Inside Components

Inside of the VPS is covered by two pieces cabinet. These two cabinets are fixed to the base cabinet with two and four screws.

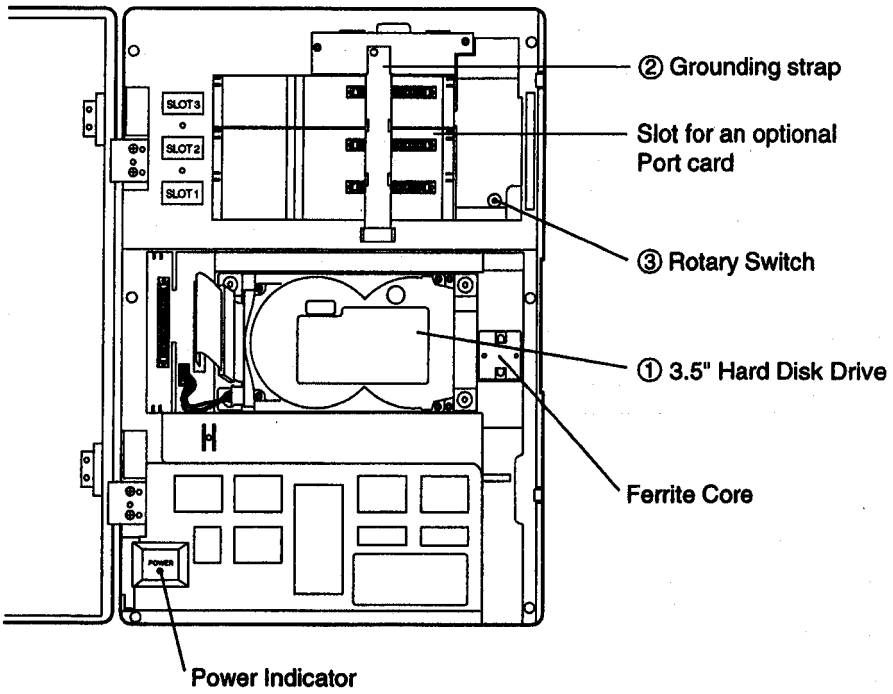


Fig. 1-3. Inside View and Components Location

① Hard Disk Drive (HDD)

The Hard Disk Drive (HDD) is installed Proprietary System Program and System Prompt. All the recorded messages from callers are stored in the HDD. The HDD is connected to CPU card using a 40 pin flat cable and 4 pin power cable.

② Grounding Strap

This Grounding Strap is an earth plate. To protect the printed circuit board from static electricity, first dischange any body static by touching the grounding Strap.

③ Rotary Switch

The Rotary Switch Provides additional function as follows. The status of this switch is checked only once after power-up. The additional functions are effective when you turn on the power after the switch changing.

Position	additional function
0	Normal Operation
1	The VPS automatically sets the RS-232C baud rate to the following parameters: baud rate 9,600 bps bit length 8 bit stop bit length 1 bit parity None In this case, the communication parameter which was programmed by the customor is ignored.
2~4	Reserved for future function.
5	The VPS initializes all of the configuration settings to default setting, and clear all of the stored messages.
6~9	Reserved for future function.

4-3. Basic Components

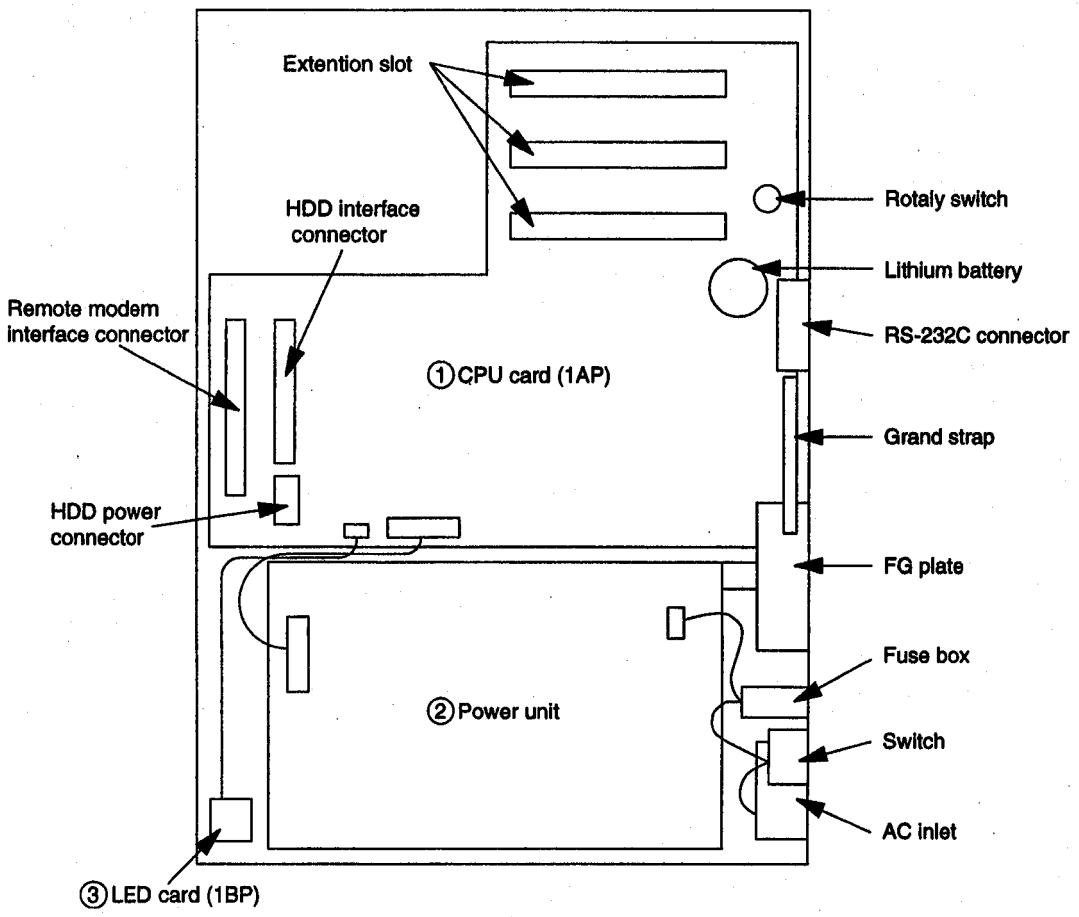


Fig. 1-4. Basic Components Location

Basic Components of VPS are CPU card, Power Card and AC Transformer. (Refer to Figure 1 - 4.)

① CPU Card (1AP)

The CPU Card is the central processing unit of the VPS. When power is on, the microprocessor (IC301) on the CPU Card runs on the ROM (IC306) based program, and executes the system initialize, self diagnostics and then an application program loading from HDD to system RAM on the CPU Card. After the program loading, CPU Card starts the incoming call service. The CPU Card allows to control the EIA232C interface and the real time clock device with back up battery. The CPU Card has 9 interface connectors as follows.

CN301 = HDD interface (40pin)
CN302 ~ CN304 =CO Card interface (50pin)
CN305 = DC power supply from power card (8pin)
CN306 = Power Indicator (LED) interface (2pin)
CN307 = EIA232C interface (25pin)
CN308 = HDD Power supply (4pin)
CN309 = Remote modem I/F connector (50pin)

② AC Power Unit

The AC power source inputs from AC inlet.
Power Source inputted from AC Transformer is rectified in Power Card, and then changed to DC +12V, to DC +5V and to DC-5V. Functions of Power Card is as follows.

- DC±5V, +12V generation.
- DC+5V back up by using large capacity capacitor.
- Power down detection.
- DC shut down control in case of abnormal condition of the voltage, current and temperature.

This power card has a variable resister (VR101) for +5V DC voltage adjustment.
DC power source generated in Power logic is supplied to CPU card via CN101.

③ LED Card (1BP)

LED Card is connected to CPU Card via CN306 and its ON/OFF states are controlled by the CPU Card.

4-4. Hardware Architecture Outline

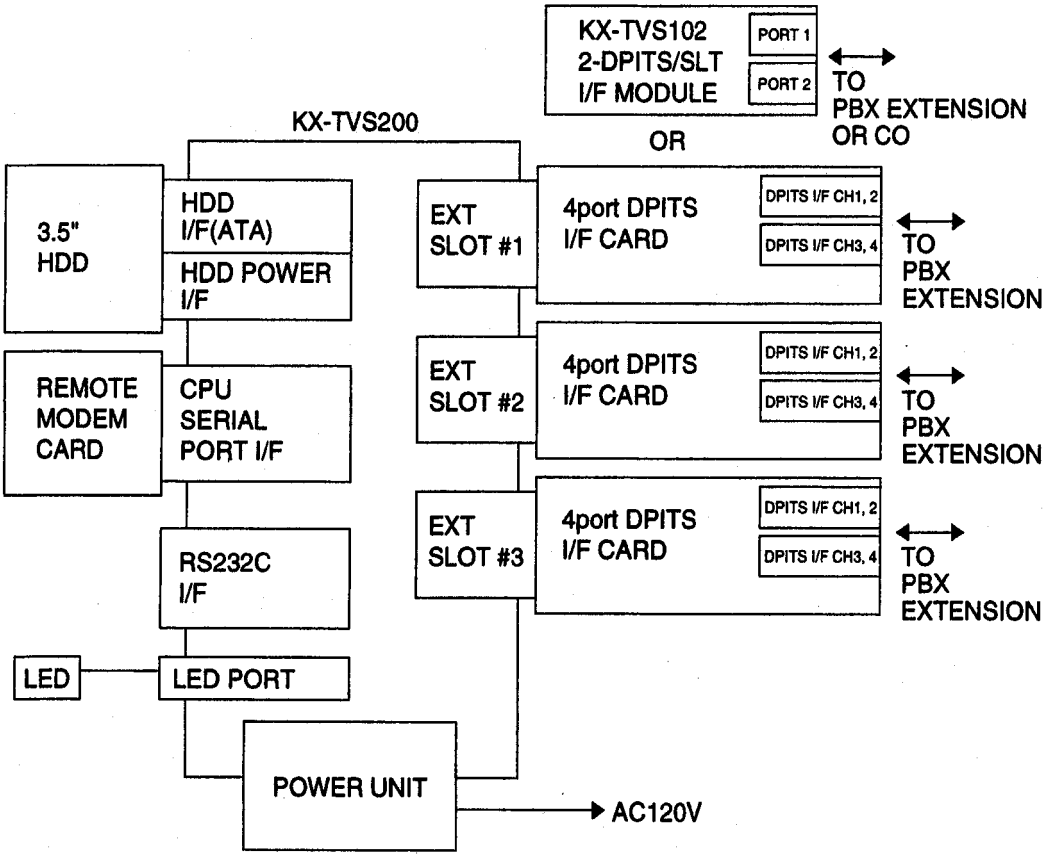


Fig. 1-5. Hardware Block Diagram

A Hardware block diagram of the VPS is shown in figure 1 - 5.
Functions of each hardware block are explained by giving an example of the process from guidance play back to message recording by Voice Mail Service.

•Bell arrival (When use KX-TVS102)

Line interface has a function to detect the bell signal inputted from Tel Jack. The 16 bit Microprocessor monitors this bell arrival through the Line Control Port periodically. When the 16 bit Microprocessor detects the bell arrival, the Microprocessor makes the line condition into an off-hook state through the line control port.

•Guidance Play back (When use KX-TVS102, KX-TVS204)

At the same time the Microprocessor transfers system prompt data stored in the HDD in advance from HDD to a voice buffer area in the system memory. (This system prompt data is compressed in half by ADPCM algorithm) The Microprocessor programs the Voice Transfer logic to the play back mode. In addition, the Microprocessor writes the play back command into FIFO on the DSP G/A. DSP monitors this FIFO periodically. If DSP receives a playback command by FIFO monitoring, DSP starts to execute ADPCM play back. In ADPCM play back the following processes are executed.

System prompt data, transfered from system memory by the voice data transfer logic , is encoded to digital voice data. In case of KX-TVS102 (then output to CODEC. The CODEC converts digital voice data to analog voice data, and outputs to the line interface.) In case of KX-TVS204 (then output to DPITS I/F.). In ADPCM play back mode, the DTMF detecting function is always activated and checks reception of the DTMF code by DSP.

•Message Recording

When DSP detects a DTMF code represented recording, it writes the DTMF code into FIFO. Microprocessor monitors this FIFO periodically. The Microprocessor receives DTMF code represented recording messages intermittently, then the Microprocessor programs Voice Data Transfer logic to Recording mode. The Message recording command is written into FIFO on the DSP card. DSP receives message recording command intermittently, DSP starts to execute ADPCM recording . In ADPCM recording, the following processes are executed. In case of KX-TVS102 (voice data input from the line interface is converted to digital voice data by CODEC DSP receives digital voice data from CODEC and executes the voice data compression based on ADPCM algorithm.). In case of KX-TVS204 (voice data input from DPITS interface is converted to PCM data by DSP ASIC • DSP receives PCM data from DSP ASIC and executes the voice data compression based on ADPCM algorithm.). DSP outputs the compressed data to Voice data transfer logic. Voice data transfer logic transmits the compressed data from DSP to system memory. Data transferred to system memory is stored in HDD by the Microprocessor. In ADPCM recording mode, DTMF detecting function, Tone detecting function, and VOX (silence) detecting function are always activated by DSP. The result of this detection is written into FIFO by DSP periodically.

•End of Message Recording disposition

The Microprocessor receives these detection results via FIFO, then detects the recording termination. (For example the conditions of termination are to receive the DTMF code representing recording finish, detect a Busy Tone or a detected silence situation more than a regulated period, etc.) When the Microprocessor detects a recording, it terminates the recording disposition then shifts over to the next step, guidance play back disposition.

The functions of the module are as follows.

•HDD	to store the voice data, and the system program.
•System memory	to store voice data temporarily, to execute the system program.
•Voice Data Transfer logic	to control the transfer of voice data between DSP to/from system memory
•DSP	voice compression/decompression (using ADPCM Algorithm).
	to detect and generate DTMF.
	to detect Tone and generate Beep Tone.
	to detect VOX (silence).
	to adjust recording level. (Automatic Recording Level Control)
•Codec	Analog to/from digital conversion of the voice data (for KX-TVS102).
•Microprocessor	controls all of the system.

INSTALLATION

1. INSTALLATION REQUIREMENTS

The VPS installation involves
- Mounting the VPS.
- Connecting PBX extensions to the VPS ports.
- Connecting a Data Terminal (VT or ASCII)
- Connecting Power to the Cabinet.
- System Programming (' Refer to Installation Manual)

Installation personnel should be familiar with the data format and change procedures of the PBX. For further explanation, refer to the "Installation Manual".

1-1. Site Requirements

Install the VPS cabinet in a dust free location. Keep it separated from other equipment that may produce heat or generate strong magnetic fields. If space permits, install the VPS in a telephone equiment room.

1-2. AC Power Requirement

It is best to power the system from a dedicated, separate circuit. If this is not possible, make sure the circuit is free of large motorized equipment, such as copy machines, and that it is protected by a fuse or circuit breaker. Make sure the power receptacle is grounded and within five feet of the cabinet.

1-3. Other Required Equipment

Each VPS port is connected via a modular line cord to a standard modular telephone jack connected to a PBX extension. Each line cord must be of sufficient length to reach between the VPS and PBX without undue stretching or tension. Keep it separated from other cords that may generate strong electric magnetic wave.
A data terminal, used for system programing, must be available at the customer site. In addition, one RS-232C cross cable is required to connect the terminal to the VPS.

The following is a list of required equipment.

Table 1-1, Installation required equipment.

Modular line Cord (male-male)	4 wire	1 cord/2 port (when connecting Panasonic KX-TD Series PBX extension)
	2 wire	1 cord/1 port (when connecting other type PBX extension)
Data Terminal (VT or ASCII)	1	
RS-232C Cross Cable	1	
Screw Driver	1	
Drill	1	

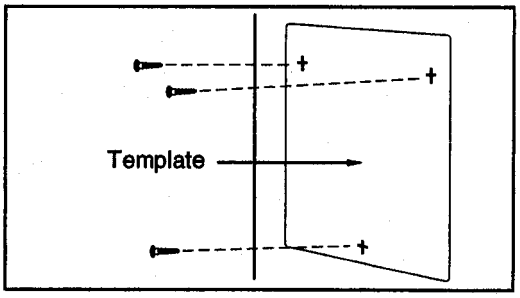
2. MOUNTING THE VPS

Mounting the VPS on the Wall

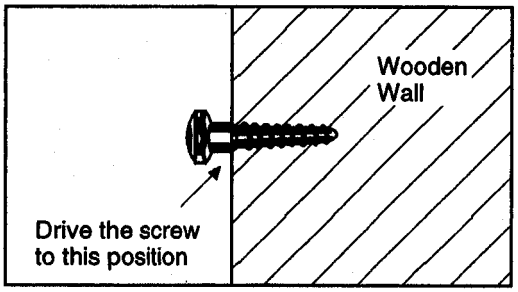
The wall where the VPS is to be mounted must be able to support the weight of the VPS. If screws other than the ones supplied are used, use the same-sized diameter screws as the enclosed ones.

To Mount on a Wooden Wall:

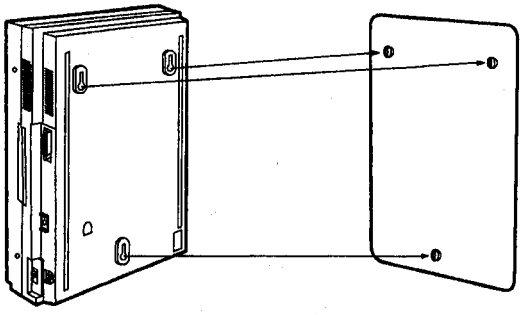
1) Place the template (included) on the wall to mark the 3 screw positions.



2) Install the 3 screws into the wall.

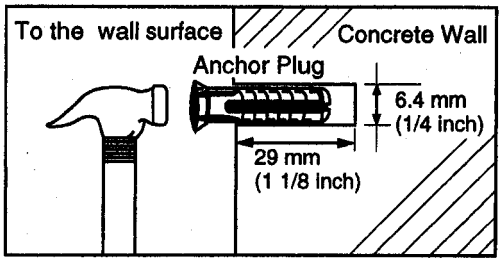


3) Hook the unit on the screw heads.

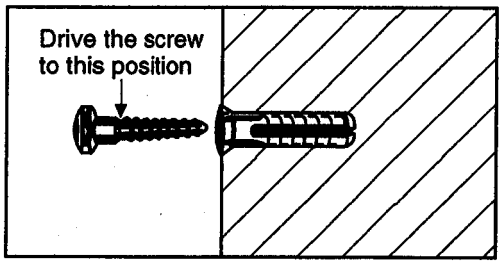


To Mount on Concrete or Mortar Walls:

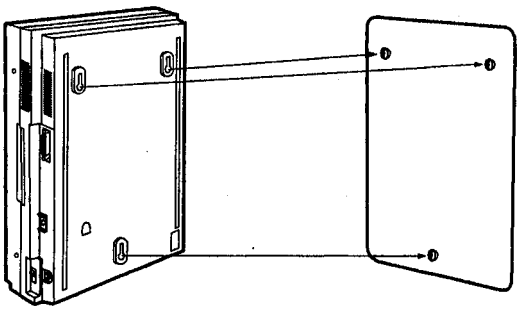
1) Place the template (included) on the wall to mark the 3 screws positions.
2) Drill 3 holes and drive the anchor plugs (included) with a hammer, flush to the wall.



3) Install the 3 screws into the anchor plugs.



4) Hook the unit on the screw heads.



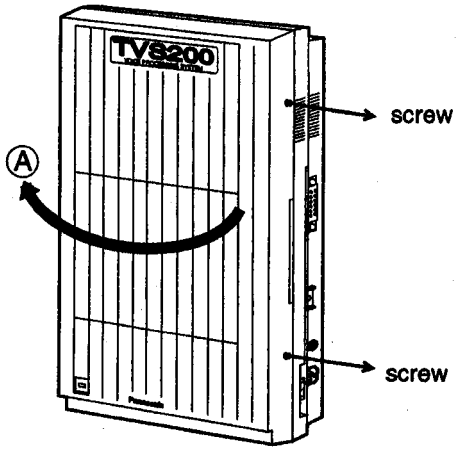
3. CONNECTING THE PBX EXTENSIONS TO THE VPS

The VPS must be connected to PBX extension lines. If you have a Panasonic KX-TD series PBX and make use of D-PITS Integration, use a 4 conductor wiring cord. If you have another type PBX, use a 2 conductor wiring cord. The maximum length of the wire varies according to your PBX type. Please refer to your PBX Installation Manual. Remember the connected extension port number on the PBX. You will call it when accessing one of the assigned incoming call services. The following models are recommended for connecting to the VPS:

- Panasonic KX-T30810
- Panasonic KX-T61610
- Panasonic KX-T123211D
- Panasonic KX-TD816
- Panasonic KX-TD1232
- Panasonic KX-T336100

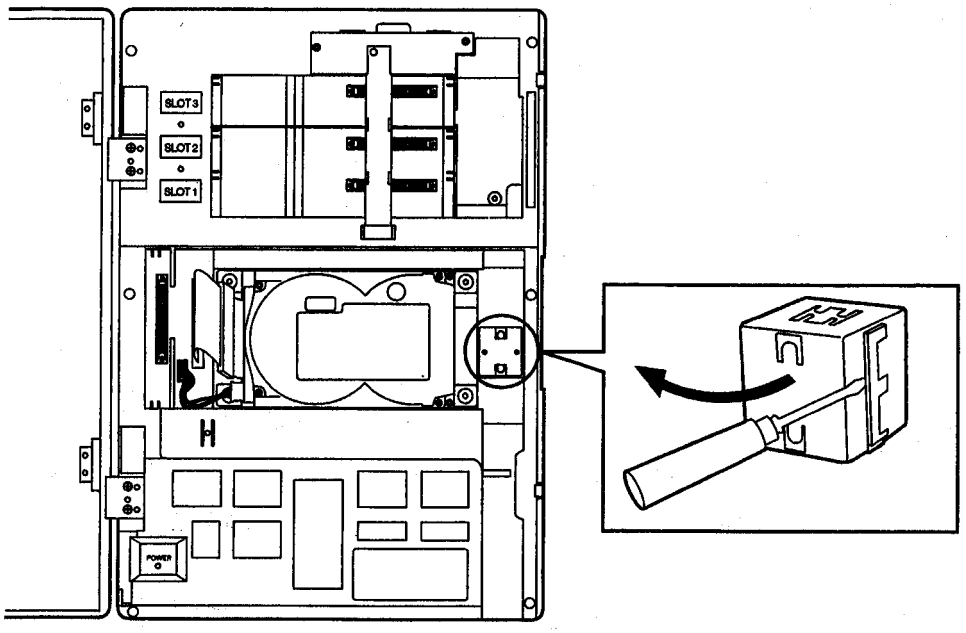
Procedure

1. Loosen two screws on the right side of the main unit, then open the front cover in the direction of arrow Ⓐ.

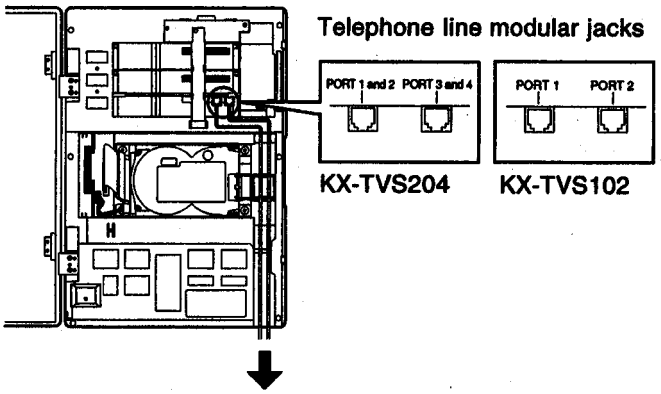


Note: The screws are attached to the front cover with springs so that they will not be lost.

2. Insert a screwdriver into the opening of the ferrite core and open it.



3. Insert the modular plug of the telephone cord into the modular jack on the Port card. Let the telephone cord through the ferrite core. Then close the ferrite core.



You can use the following two kinds of Port cards in the KX-TVS200.
(No port cards are installed at the factory.)

- 4 Digital ports expansion card (KX-TVS204)
- 2 Digital/Analog ports expansion card (KX-TVS102)

• One KX-TVS204 (2 jacks) can support four VPS ports using D-PITS Integration mode only, and KX-TVS204 does not work under other integration modes (INBAND Integration, None).

• One KX-TVS102 (2 jacks) can support two VPS ports under any integration mode.

The Number of Ports VPS Cards can support

Card Type	Integration Mode	
	D-PITS	Inband/None
KX-TVS204	4	Not available
KX-TVS102	2	2

Note: You can use only one Integration mode among D-PITS, Inband, and None. To set the Integration mode, please see "4.5.6.3.1 Dialing Parameters". (Refer to Installation Manual)

• There are three SLOTs in the KX-TVS200, and 4 VPS ports are assigned physically for each SLOT, so 12 VPS ports are physically prepared in total, however system can support only 8 ports max.
But in case you use the KX-TVS102, only the first 2 ports of the physical 4 ports of the card will be effective.
For example, when you mount the KX-TVS204 in SLOT1, the VPS supports Port 1-4. But when you mount the KX-TVS102 in SLOT1, the VPS supports only Port1 and Port2. Please see the following table for all card configurations and the effective number of ports in each case. When the VPS administrator sets up parameters for any port ["4.5.3 Port Service" and "4.5.6.2 Hardware-Port Setting Refer to Installation Manual"], please be careful to set up for the proper port number of VPS ports.

Card Configuration (D-PITS Integration)

Pattern No.	SLOT 1 (Port 1,2,3,4)	SLOT 2 (Port 5,6,7,8)	SLOT 3 (Port 9,10,11,12)	Total Number of Ports
1	TVS204 (Port 1,2,3,4)			4
2		TVS204 (Port 5,6,7,8)		4
3			TVS204 (Port 9,10,11,12)	4
4	TVS204 (Port 1,2,3,4)	TVS204 (Port 5,6,7,8)		8
5	TVS204 (Port 1,2,3,4)		TVS204 (Port 9,10,11,12)	8
6		TVS204 (Port 5,6,7,8)	TVS204 (Port 9,10,11,12)	8
7	TVS204 (Port 1,2,3,4)	TVS102 (Port 5,6)		6
8	TVS204 (Port 1,2,3,4)		TVS102 (Port 9,10)	6
9	TVS204 (Port 1,2,3,4)	TVS102 (Port 5,6)	TVS102 (Port 9,10)	8
10	TVS102 (Port 1,2)	TVS204 (Port 5,6,7,8)		6
11		TVS204 (Port 5,6,7,8)	TVS102 (Port 9,10)	6
12	TVS102 (Port 1,2)	TVS204 (Port 5,6,7,8)	TVS102 (Port 9,10)	8
13	TVS102 (Port 1,2)		TVS204 (Port 9,10,11,12)	6
14		TVS102 (Port 5,6)	TVS204 (Port 9,10,11,12)	6
15	TVS102 (Port 1,2)	TVS102 (Port 5,6)	TVS204 (Port 9,10,11,12)	8
16	TVS102 (Port 1,2)			2
17		TVS102 (Port 5,6)		2
18			TVS102 (Port 9,10)	2

Pattern No.	SLOT 1 (Port 1,2,3,4)	SLOT 2 (Port 5,6,7,8)	SLOT 3 (Port 9,10,11,12)	Total Number of Ports
19	TVS102 (Port 1,2)	TVS102 (Port 5,6)		4
20	TVS102 (Port 1,2)		TVS102 (Port 9,10)	4
21		TVS102 (Port 5,6)	TVS102 (Port 9,10)	4
22	TVS102 (Port 1,2)	TVS102 (Port 5,6)	TVS102 (Port 9,10)	6

Card Configuration (non D-PITS Integration)

Pattern No.	SLOT 1 (Port 1,2,3,4)	SLOT 2 (Port 5,6,7,8)	SLOT 3 (Port 9,10,11,12)	Total Number of Ports
1	TVS102 (Port 1,2)			2
2		TVS102 (Port 5,6)		2
3			TVS102 (Port 9,10)	2
4	TVS102 (Port 1,2)	TVS102 (Port 5,6)		4
5	TVS102 (Port 1,2)		TVS102 (Port 9,10)	4
6		TVS102 (Port 5,6)	TVS102 (Port 9,10)	4
7	TVS102 (Port 1,2)	TVS102 (Port 5,6)	TVS102 (Port 9,10)	6

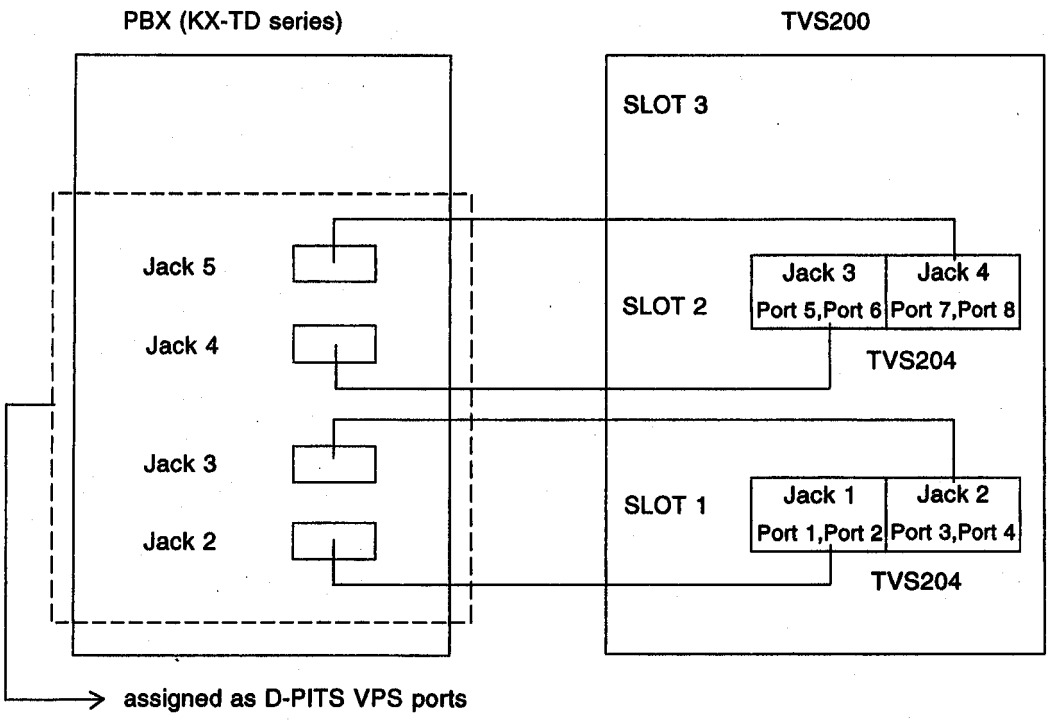
- In conclusion, the KX-TVS200 can support a maximum of 8 ports in D- PITS Integration mode and a maximum of 6 ports in non D-PITS Integration mode.

D-PITS Integration

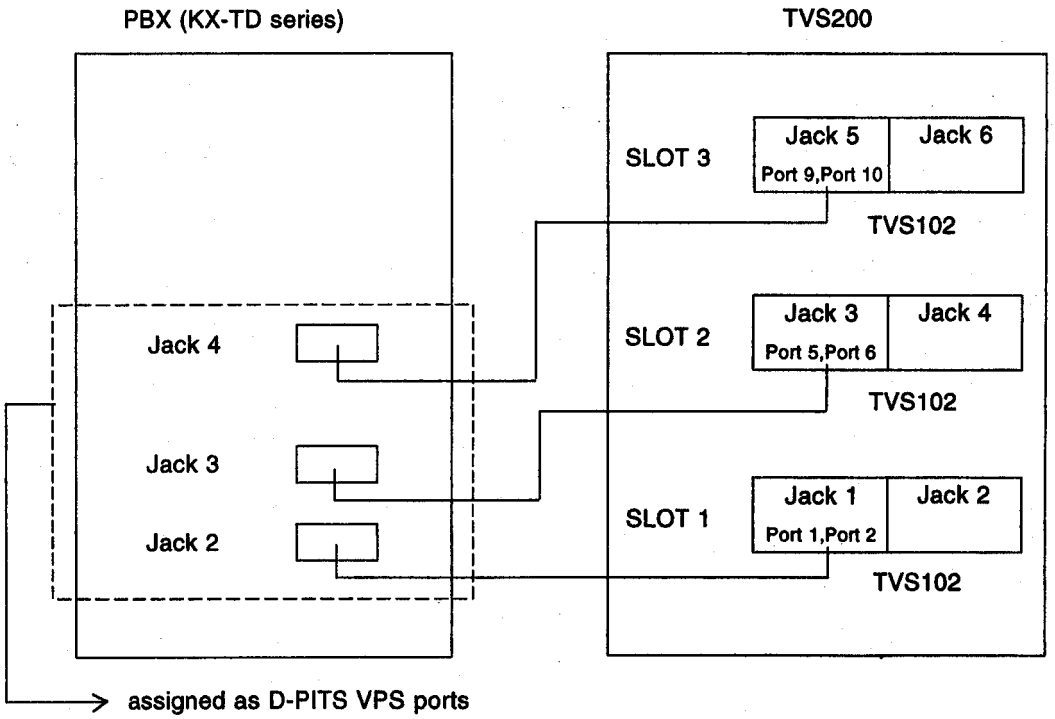
To the Panasonic KX-TD series PBX, the VPS ports look like digital extensions.
The digital communication (2B+D) provides two VPS ports for each Digital Station port of the PBX.
For example, when you mount two KX-TVS204 cards, you can use eight VPS ports in total by connecting four jacks of the KX-TD1232 to four jacks of the KX-TVS200.

Note: 1. To use D-PITS Integration, the lowest jack of the KX-TVS200 must be connected to the lowest number jack assigned as a Voice Mail Port Assignment in KX-TD series. Please see the following connection examples.

Connection Example (KX-TVS204×2)



Connection Example (KX-TVS102×3, D-PITS Integration Mode)

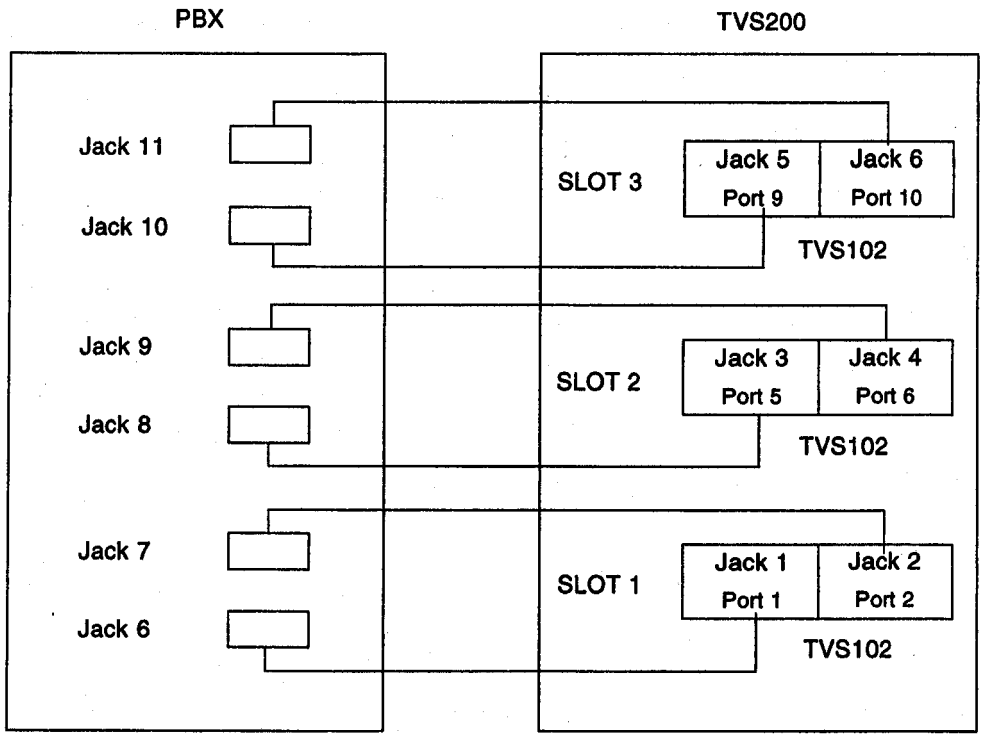


2. To communicate between the VPS and the PBX through D-PITS Integration, the PBX and VPS must be programmed to work together.
   Please refer to "4.5.6.3.1 Dialing Parameters" (Refer to Installation Manual) about the VPS setting of Integration Mode, and please refer to the Installation Manual of Panasonic KX-TD series regarding "Voice Mail Port Assignment" on the PBX side.

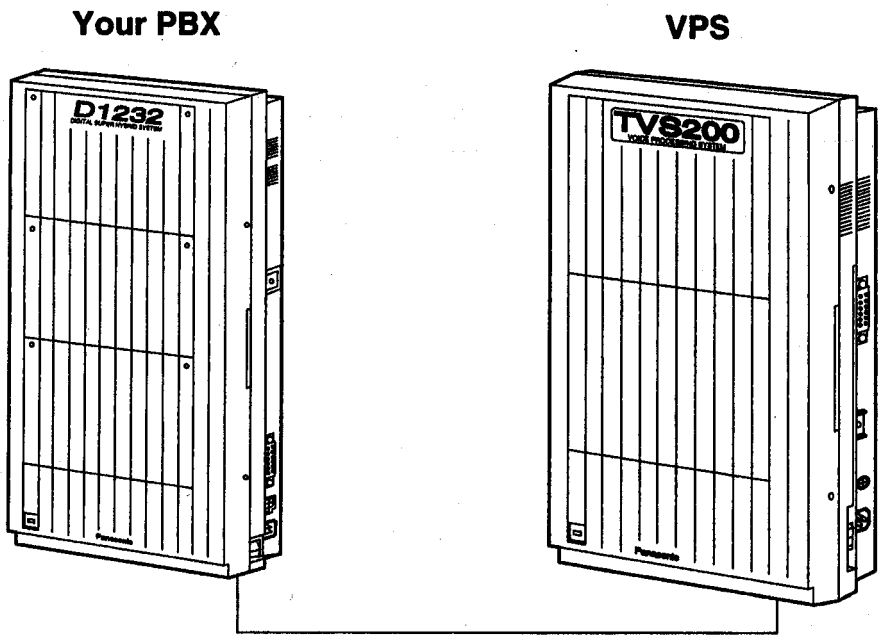
● **Inband/None Integration**

To the PBX, the VPS looks like SLT sets through standard single-line(tip/ring) telephone interfaces. Please see the following connection example.

Connection Example (KX-TVS102×3, Inband/None Integration Mode)



3. Connect the telephone line to the extension port of the PBX by following instructions below.



4. Close the front cover of the VPS system (and PBX if the cover is removed).
   Reverse the procedure of step 1.
5. Tighten the two screw firmly.
   Reverse the procedure of step 1.

4. CONNECTING A DATA TERMINAL

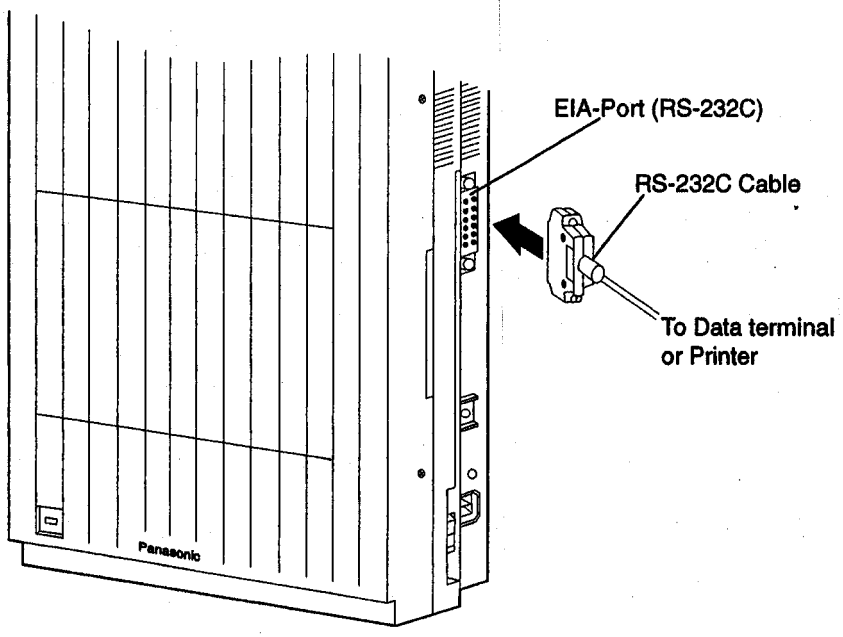
For the system administration (system set-up, mailbox setup, and system diagnosis), the VT 100 or ASCII terminal must be connected to a serial interface (EIA port) of the VPS. If using DEC VT100 or VT100 compatible terminal, the system administrator program provides the conversational menu-driven environment. If you wish to output reports to a printer, also connect to the VPS and the printer using the EIA port. The wiring and parameters are the same as those for a terminal. The default communication parameters of the VPS are shown as follows.

RS-232C parameters

- Baud Rate: 9600 bps
- Word Bit Length: 8 bits
- Parity: None
- Stop Bit Length: 1 bit

Connecting RS-232C cable

Precaution Before connecting the cable, make sure to turn off the power switch on both data terminals and the VPS.



Insert the RS-232C cable into the VPS with the connector indicating the same direction.

Printer Connection

1. Make cables so that the printer may be connected to the VPS as shown in the following chart. Cable must be shielded and the maximum length is 2m (6.5 feet).

Connection Chart:

EIA (RS-232C) port on the VPS			EIA (RS-232C) port on the Printer		
Circuit Type (EIA)	Signal Name	Pin No.	Pin No.	Signal Name	Circuit Type (EIA)
AA	FG	1	1	FG	AA
BA	TXD	2	3	RXD	BB
BB	RXD	3	2	TXD	BA
AB	SG	7	20	DTR	CD
CD	DTR	20	7	SG	AB
			5	CTS	CB
			6	DSR	CC
			8	DCD	CF

The pin configuration of the EIA (RS-232C) connector is as follows.

Pin No.	Signal Name		Circuit Type	
			EIA	CCITT
1	FG	Frame Ground	AA	101
2	TXD	Transmitted Data	BA	103
3	RXD	Received Data	BB	104
4	RTS	Sound	CA	105
6	DSR	Ready	CC	107
7	SG	Signal Ground Data Carrier	AB	102
8	DCD	Defect	CF	109
20	DTR	Data Terminal Ready	CD	108.2

(Reference)
EIA (RS-232C)
SIGNALS

Frame Ground (FG)
Connects to the unit frame and the earth ground conductor of the AC power cord.

Transmitted Data (TXD) ..... (output)
Conveys signals from the unit to the printer (or terminal). A "Mark" condition is held unless data or BREAK signals are being transmitted.

Received Data (RXD) ..... (input)
Conveys signals from the printer (or terminal).

Reguest To Send (RTS) ..... (output)
This lead is held on whenever DSR is on.

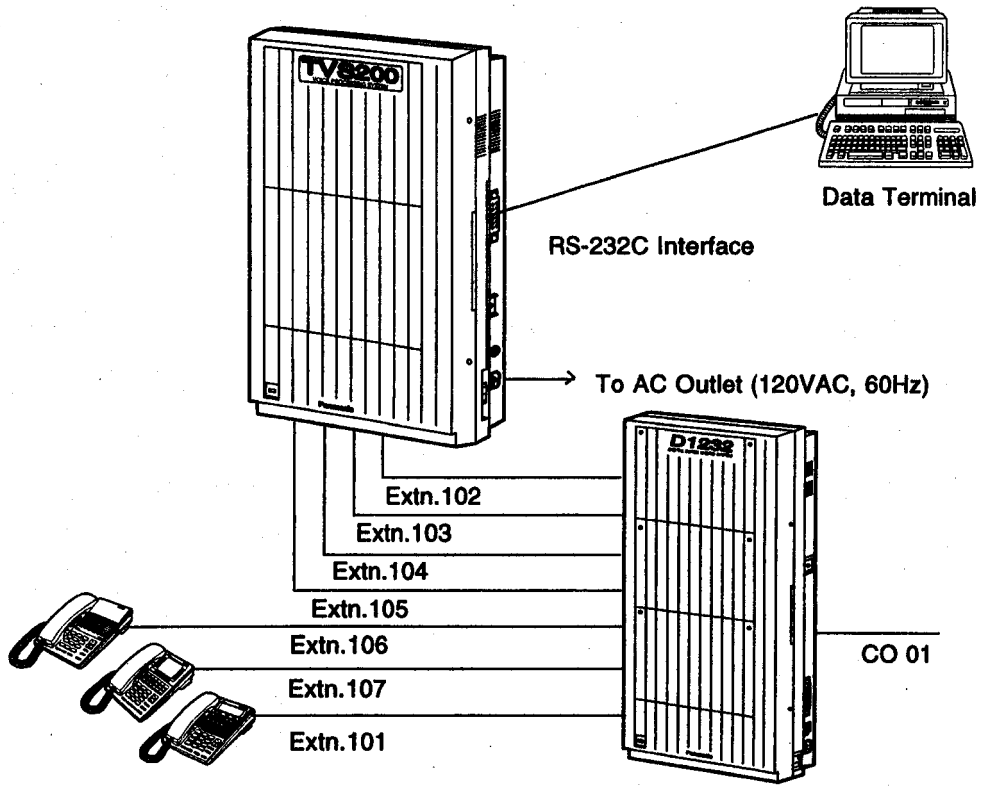
Signal Ground (SG)
Connects to the DC ground of the unit for all interface signals.

Data Terminal Ready (DTR) ..... (output)
This signal line is turned ON by the unit to indicate that it is ON LINE. Circuit DTR ON does not indicate that communication has been established with the printer (or terminal). It is switched OFF when the unit is OFF LINE.

5. POWER CABLE CONNECTION

Attach the AC jack at the cord to AC inlet of the VPS.
Before connecting the power cable to an AC outlet, make sure all other connections (RS-232C data terminal with VPS, PBX with VPS, PBX with telephone lines) are secure, and front cover is closed firmly. Use the AC outlet dedicated to the VPS unit.

Example:



6. SYSTEM PROGRAMMING

For the details of the system programming, refer to "Installation Manual".

7. STARTING THE SYSTEM

Turn on the power switch, the VPS will start up in the following sequence.

FOR KX-TVS102×3

```
CARD TEST ...
SYSTEM SETUP ...
  1..   2..   3..   4..   5..   6..   7..   8..   9..   10..
 11..  12..  13..  14..

  Active COs     :  1  2    5  6  9  10
 DPIT Interface connection is Established
** ON LINE MODE **
>
```

FOR KX-TVS204×2

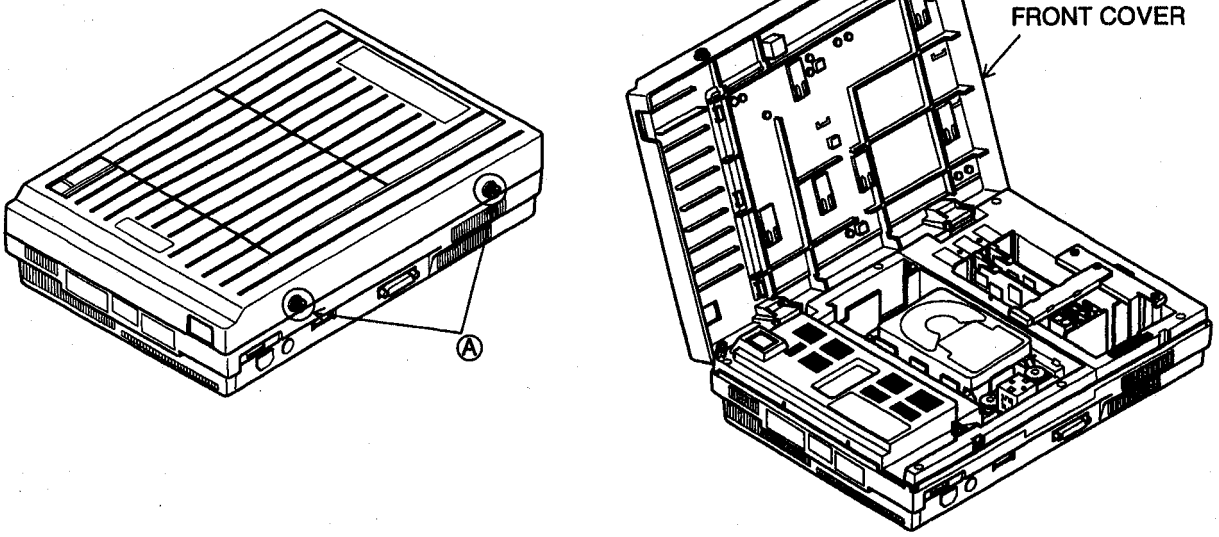
```
CARD TEST ...
SYSTEM SETUP ...
  1..   2..   3..   4..   5..   6..   7..   8..   9..   10..
 11..  12..  13..  14..

  Active COs     :  1  2  3  4  5  6  7  8
 DPITS Interface Connection is Established
** ON LINE MODE **
>
```

MEMO

DISASSEMBLY INSTRUCTIONS

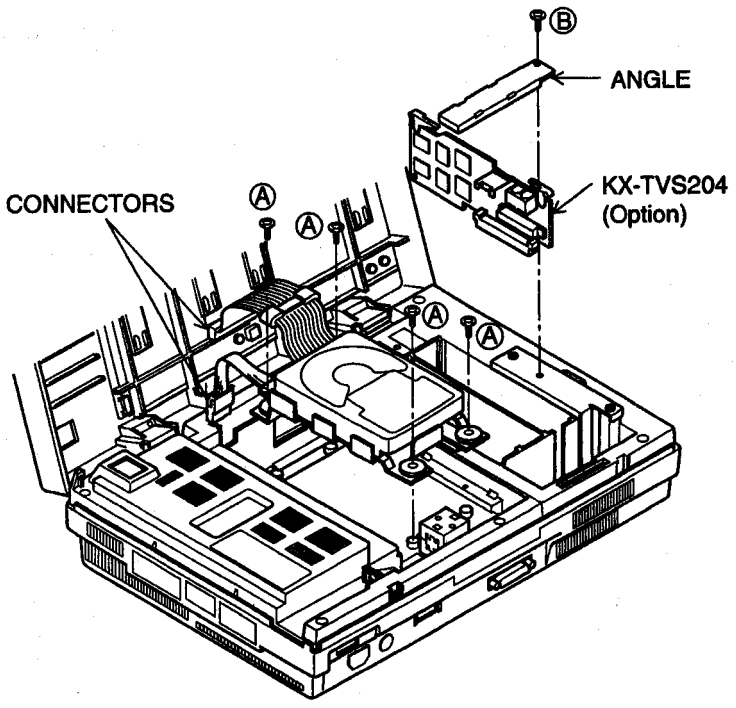
Ref. No. 1	HOW TO REMOVE THE FRONT COVER
Procedure 1	

1. Loosen the two screws (A).
2. Open the front cover.
3. Slide the front cover in the direction of the arrow when removing it.



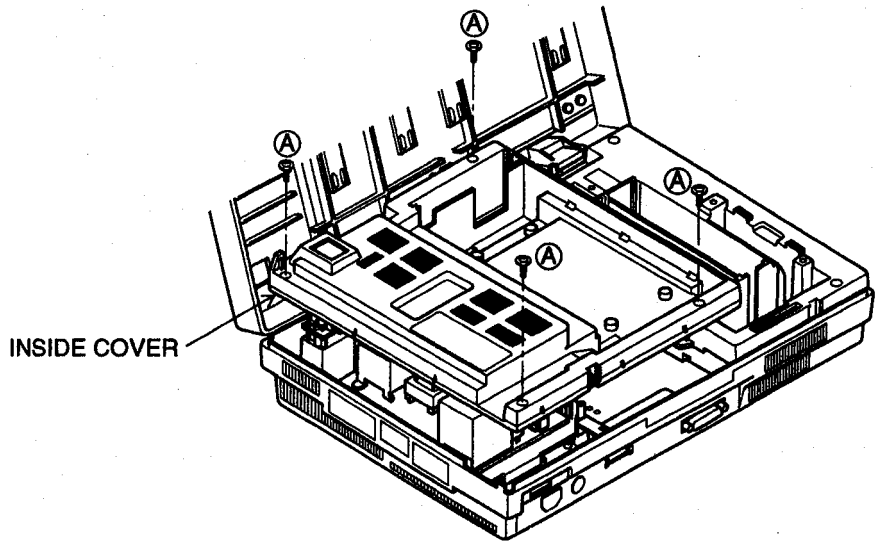
Ref. No. 2	HOW TO REMOVE THE HARD DISK DRIVE UNIT AND KX-TVS204
Procedure 1 → 2	

1. Remove the four screws Ⓐ.
2. Pull out the two connectors.
3. Remove the Hard Disk Drive Unit.
4. Remove the screws Ⓑ.
5. Remove the angle
6. Remove the KX-TVS204



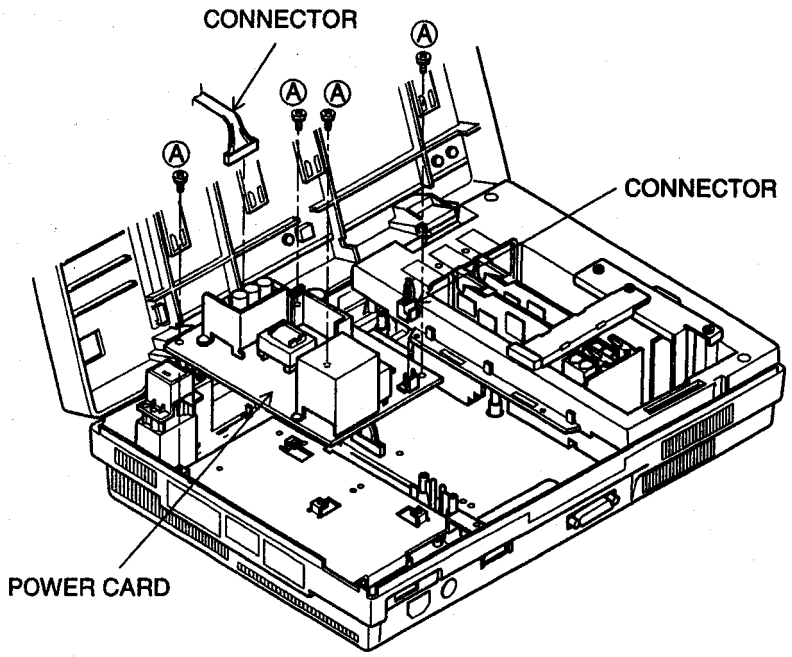
Ref. No.3	HOW TO REMOVE THE FRONT COVER
Procedure 1 → 2 → 3	

1. Remove the Hard Disk Drive Unit. (Refer to Ref. No.2)
2. Remove the four screws Ⓐ.
3. Remove the inside cover.



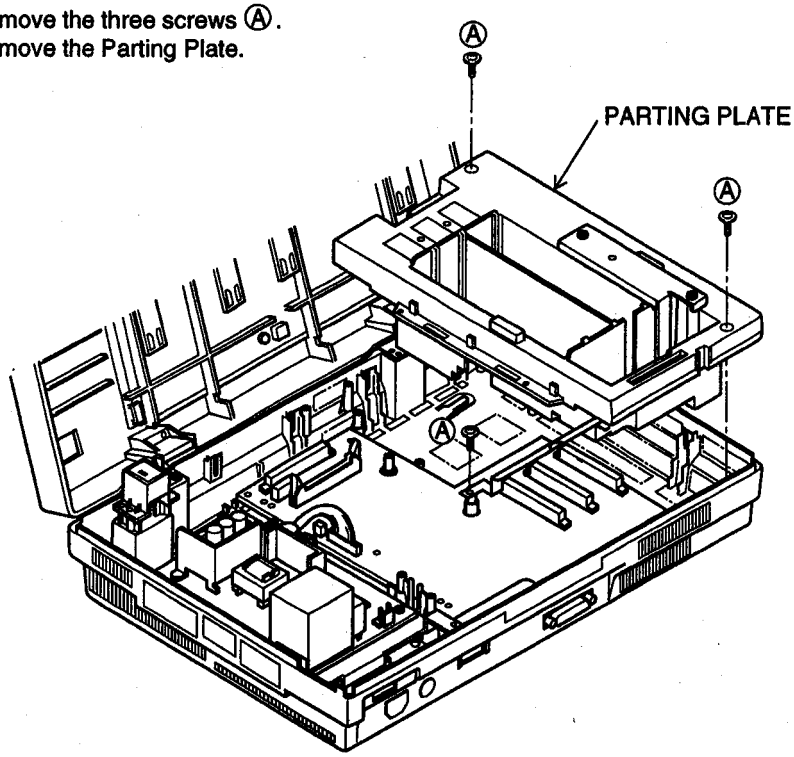
Ref. No. 4	HOW TO REMOVE THE POWER CARD
Procedure 1 → 2 → 3 → 4	

1. Remove the four screws Ⓐ.
2. Remove the two connectors.
3. Remove the Power Card.



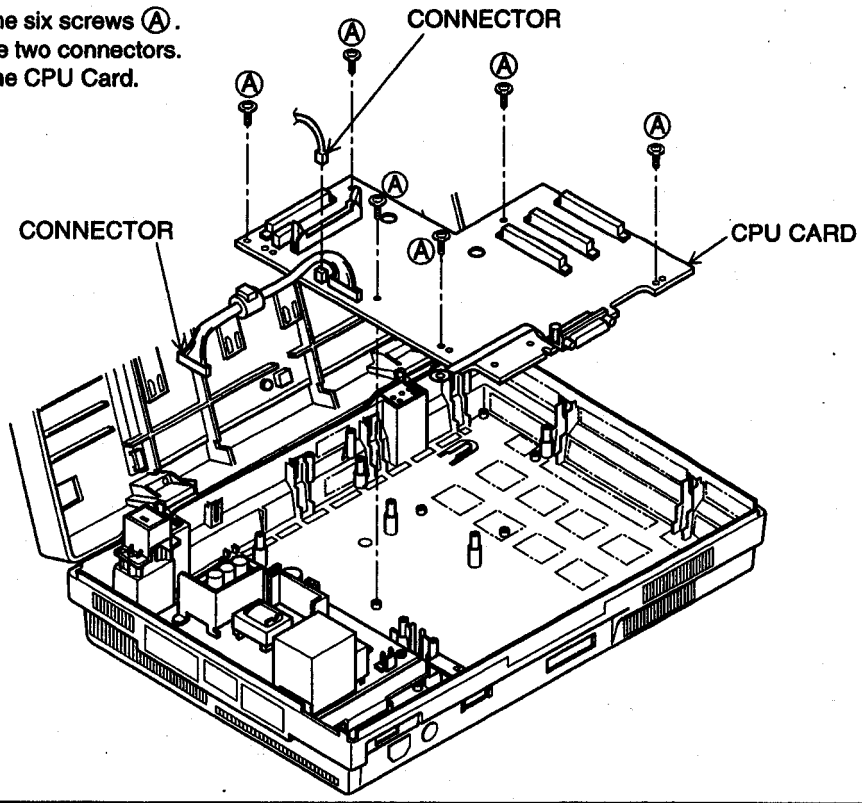
Ref. No. 5	HOW TO REMOVE THE PARTING PLATE
Procedure 1 → 2 → 3 → 5	

1. Remove the three screws Ⓐ.
2. Remove the Parting Plate.



Ref. No. 6	HOW TO REMOVE THE CPU CARD
Procedure 1 → 2 → 3 → 5 → 6	

1. Remove the six screws Ⓐ.
2. Pull out the two connectors.
3. Remove the CPU Card.



HOW TO REPLACE FLAT PACKAGE IC

■ PREPARATION

· SOLDER - - - - - - - - Sparkle Solder 115A-1, 115B-1
OR
Almit Solder KR-19, KR-19RMA

· Soldering iron - - - - - - Recommended power is 30 W to 40 W.
Temperature of Copper Rod 662 ± 50 °F (350 ±10 °C)

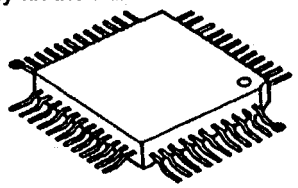
(An expert may handle 60~80 W iron, but a beginner might damage the foil by overheating.)

· Flux - - - - - - - - - - - HI115 Specific gravity 0.863

(Original flux will be replaced daily.)

■ PROCEDURE

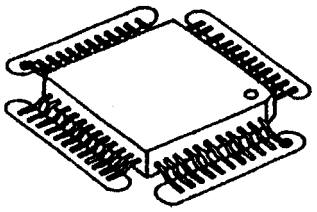
1. Temporarily fix the FLAT PACKAGE IC by soldering two marked pins.



●..... Temporary soldering point.

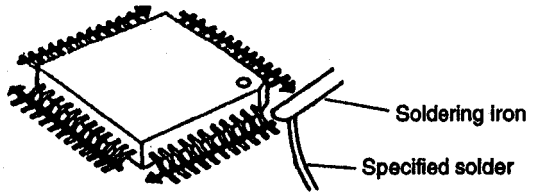
*Most important matter is accurate setting of IC to the corresponding soldering foil.

2. Apply flux to the all pins of the FLAT PACKAGE IC.



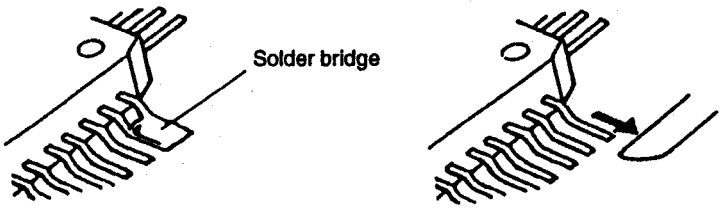
..... Flux

3. Solder the specified solder in the direction of the arrow, while sliding the soldering iron.



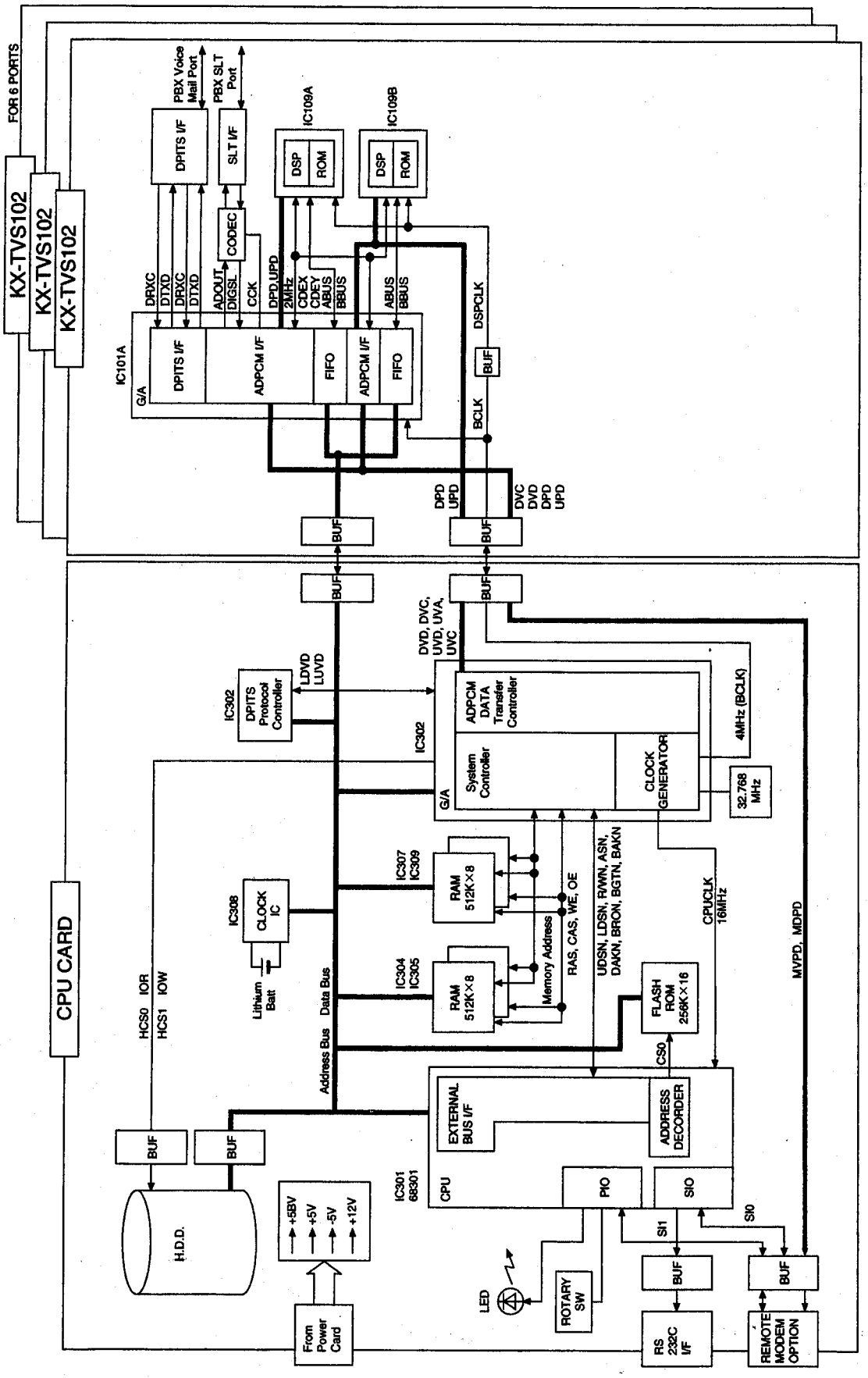
■ MODIFICATION PROCEDURE OF SOLDER BRIDGE

1. Re-solder slightly on bridged portion.
2. Remove any remaining solder along the pins using a soldering iron as shown below.



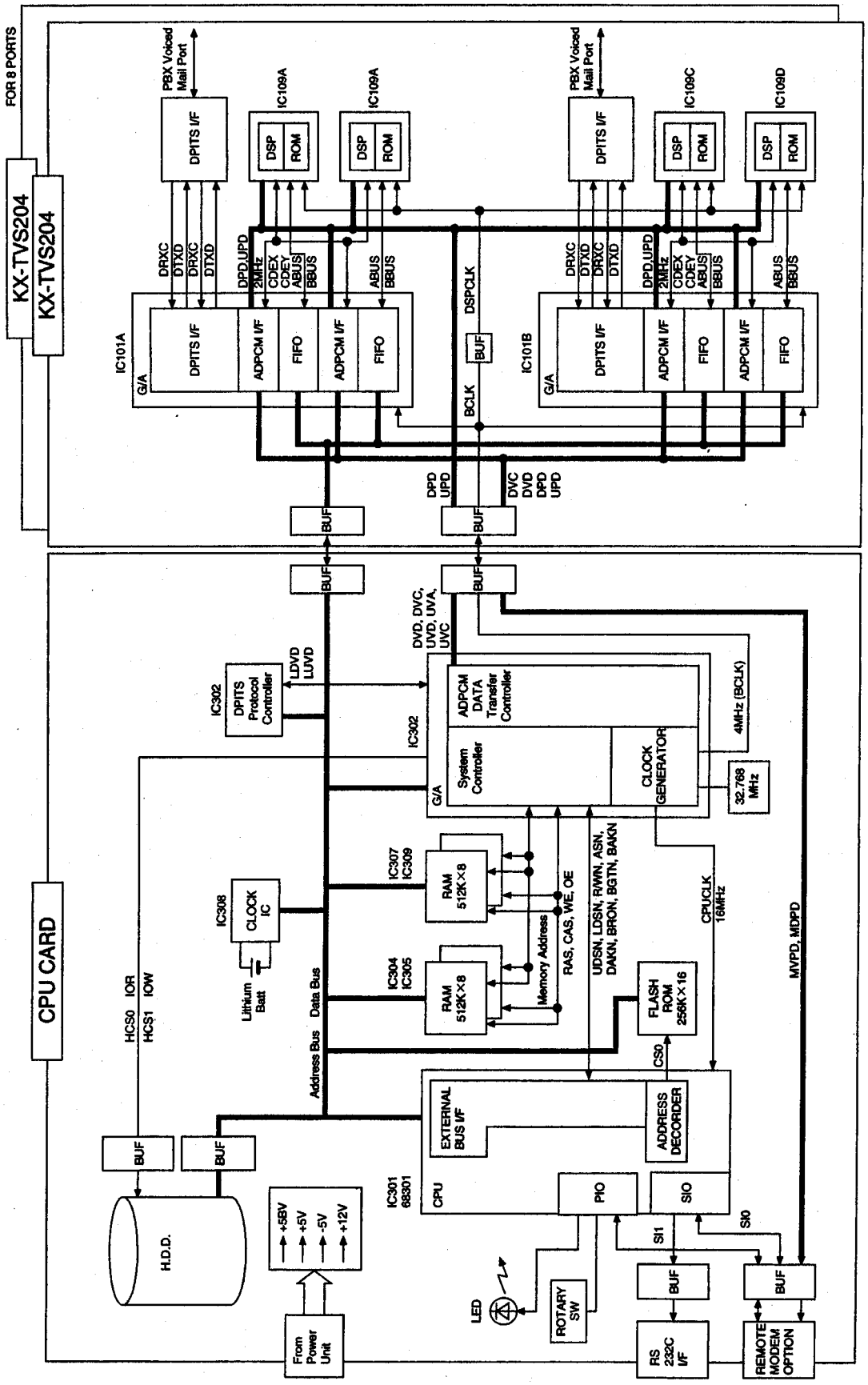
SYSTEM BLOCK DIAGRAM

(Installed 3-KX-TVS102 cards)



FUNCTIONAL BLOCK DIAGRAM

(Installed 2-KX-TVS204 cards)



1. SYSTEM SPECIFICATIONS

The Table 3-1 shows the System Specifications.

Table 3-1. SYSTEM SPECIFICATIONS

ITEM	DESCRIPTIONS	
Cabinet	Wall mounted type stand-alone style	
Dimension (H × W × D)	468 × 327 × 101 mm (18-7/16" × 12-7/8" × 4")	
Weight	5.3 kg	
Power Source	AC 120 V, 60 Hz	
Voice Storage Capacity	32 hours	
Line Capacity Line connector Line interface	KX-TVS102 Basic 0 ports (maximum 6 ports) 4 pin moduler jack type connector Port-A: D-PITS/SLT Hybrid interface Port-B: SLT interface	KX-TVS204 Basic 0 ports (maximam 8 ports) 4 pin modular jack type connector Port-A : CH1, CH2 D-PITS I/F Port-B : CH3, CH4 D-PITS I/F
Data Terminal Interface	Asynchronous RS-232C Port (25 pin Dsub connector) × 1 Data Rate: 300 up to 19,200BPS (programmable)	
Operation Switches	Power Switch × 1 Mode Configuration Switch × 1 (only maintenance use)	
LED	Power Indicator (red) × 1	
Dialling Method	Tone duration/Pulse (10/20 pps)	
Flash time	100/300/600/900 msec (programmable)	
CPC detection	None/6.5/150/300/450/600 msec (programmable)	
Extension numbering	2 to 5 digits (programmable)	
Pause time	1 to 9 sec (programmable)	
Message Waiting Lamp	Programmable DTMF sequence, or D-PITS data line	
Number of Mailboxes	maximum 1024	
Number of Messages	100 per mailbox (programmable)	
Personal Greeting Message Length	8 to 60 sec (programmable)	
Message Retention Time	New: 1 to 30 days Old: 1 to 30 day or unlimited	
Message Length	1 to 6 min (programmable)	
Reports output	Mailbox list, Class of Service list, System Service report, Call Account report, Port Usage report, Mailbox Usage report, FAX report	

2. CPU CARD

The CPU card serves as the main controller of the KX-TVS200, and it incorporates a CPU (TMP68301/16 MHz: IC301) which is 68HC000-compatible. This CPU comes with a built-in serial port (RS-232C), parallel port, timer and interrupt controller.

Installed as the base memory are a 4M-bit flash ROM (IC308) and 2MB RAM (IC304/305/307/309). The system initialize program, self-diagnosis execution program and the program for booting the system from the hard drive are stored in the ROM. The RAM is used for system program execution and voice buffer purposes.

A calendar IC (IC308) which is backed up by a battery is mounted on this card to provide time information.

The following external interfaces are provided: an IDE type hard disk interface (1 slot) enabling up to 2 units to be controlled, an asynchronous communication RS-232C interface (1 port) supporting transfer rates up to 19.2 kbps, an I/O card expansion bus (3 slots: CN302/303/304) for connecting existing line interface module KX-TVS102 and 4-port DPITS interface cards, and an expansion serial interface (1 slot: CN309) for connecting a remote modem.

The expansion bus for connecting the line interface consists of an 8-bit slave I/O bus and a DMA data transferable serial voice channel bus. The serial voice channel bus is an original bus which is capable of transferring 3 kinds of serial data for 32 channels. The transfer data includes PCM data (max. 64 kbps: DPD and UPD signals), voice data (max. 32 kbps: UVD and DVD signals), and PITS data (max. 32 kbps: UVA, UVC and DVC signals). The PCM data is connected to the remote modem interface, and after it has been restored to analog signals on the remote modem card, it is supplied to the modem IC to enable modem transmission. DMA transfer of the voice data with the main memory is enabled by combining it with the DMA channel.

The KX-TVS200 accommodates three 4-port DPITS cards and three KX-TVS102 modules which can be installed in its expansion slots. Its port expandability extends up to 12 ports for the 4-port DPITS cards and up to 6 ports for the KX-TVS102 modules.

The remote modem interface is an asynchronous communication serial interface with full specifications. It has 2-bit mode switching signals, 2-bit test mode switching signals and PCM data input and output signals. The interface enables modem communication at up to 14.4 kbps at the lowest port number assigned to the expansion slots. The port used for communication can be selected by the mode switching signal (for each slot).

Table 3-2. SPECIFICATIONS OF THE CPU CARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
CPU	68EC000 compatible	Running frequency : 16.384 MHz (IC301)
RAM	2.0M byte	4Mbit Dynamic RAM × 4 (IC304/IC305/IC307/IC309)
ROM	512k byte	4Mbit Flash ROM × 1 (IC306)
INTERRUPT CONTROLLER	10 levels	hardware interrupt request notify to CPU (IC301)
TIMER	3 Channels	for using the system management (IC301)
RS-232C I/F	1 Channels	Asynchronous (300 - 19.2kBPS) (IC301)
Pararell I/O Port	13 bits	for using LED on/off, Rotary Switch sensing (IC301)
D-PITS I/F	CCITT X.25 Level-2	D-PITS Protocol Control (IC303)
System Controller	Custom LSI	for the all of the system timing control (IC302)
CLOCK	Real Time Clock	with Battery Backup (IC308)
HDD I/F	40pin connector × 1 4 pin connector × 1	connecting upto 2 Hard Disk Drives (IC301)
EXP. SLOT	50pin connector × 3	connecting DSP/COL module (IC302 to CN304)

2.1 SPECIFICATIONS TABLE

BLOCK	SPECIFICATIONS	DESCRIPTIONS
CPU	68HC000 compatible	Running frequency : 16.384MHZ
ROM	512Kbyte	4Mbit Flash ROM X 1chip (256k X 16)
INTERRUPPT CONTROLLER	10Level	#0:INTO (active Low / Level mode)
		#1:IDE-HDD (active High / Level mode)
		#2:DMA-VCH(active Low/ Level mode)
		#3:Serial interface #0(for Remote modem)
		#4:Serial interface #1(for RS-232C#0)
		#5:DPITS-HDLC
		#6:W.D.T.(active Low / Level mode)
		#7:Fax card int(active Low / Level mode)
		#8:not use (Serial I/F #0 DSR signal)
		#9:not use (Serial I/F #0 DTR signal)
TIMERs	3 Channels	base clock=16.384MHz (= CPU clock)
RS-232C I/F	1 Channels	RS-232C Async. only (300-19.2bps)
Pararell IO	13 Bits	bit 12: Watch dog timer int
		bit 11: D.C. Alarm detect (0:power down)
		bit 10: modem control signal#1
		bit 9: modem control signal#0
		bit 8: modem u law /a law control
		bit 7: Rotaly Switch 3
		bit 6: Rotaly Switch 2
		bit 5: Rotaly Switch 1
		bit 4: Rotaly Switch 0
		bit 3: modem mode select #1
		bit 2: modem mode select #0
		bit 1: not use
		bit 0: RUN LED (1:LED on)
DPITS cont.	MT8952B HDLC LSI	CCITT X.25 Level-Commpatible Date
Voice cont.	VOICE-CH Controller	DMA controled 32 Voice Channel
Watch Dog	1 channel	HOST CPU Hang up Protection
Clock	MSM6242B	Battery Backuped Real Time Clock
HDD I/F	IDE interface	40pin IDE connector X 1 +5V,+12V POWER CONNECTOR X 1

2. 2 RS-232C INTERFACE

The TMP68301 has a separate 3-channel serial interface which supports full duplex asynchronous communication (UART). In the KX-TVS200, channel 0 is used as the remote modem interface and channel 1 as the existing RS-232C interface. Since channel 2 is not used, it is initialized only.

In terms of channel 0, modem control logic has been loaded, and CTS (clear to send), DSR (data set ready), DTR (data terminal ready) and RTS (request to send) control is added. For further details on the remote modem interface using this channel, refer to the next section.

Channel 1 is used as the existing RS-232C interface and controlled only by the TXD and RXD data send/receive signals. It is connected to the 25-pin D-sub connector as indicated below.

2. 3 REMOTO MODEM INTERFACE

The KX-TVS200 has a remote modem interface which uses serial I/O channel #0 of the CPU.

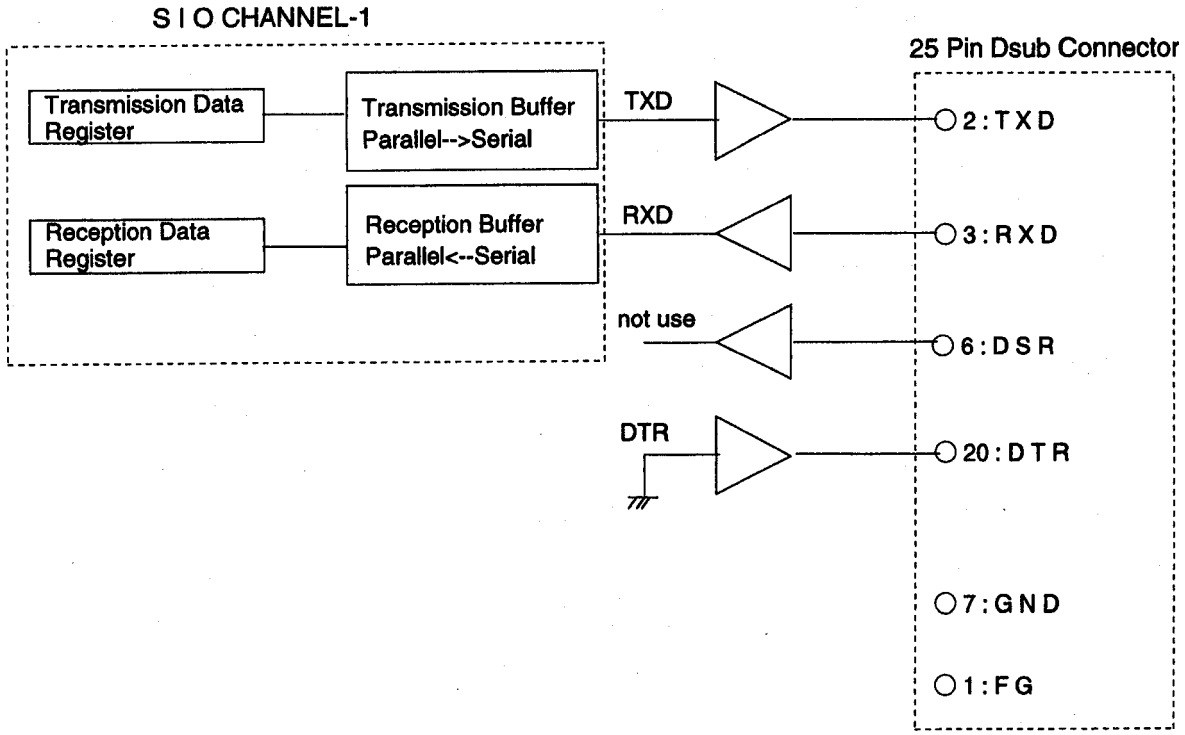
It is controlled by part of the serial interface and parallel interface of the host CPU.

The voice data of the PCM voice data highway, which is supplied to the CPU circuit board from the KX-TVS102 or KX-TVS204 line module, is converted into analog signals by the codec on the modem card and input to the modem IC.

The modem IC converts the modem signals into data using the modem communication protocol supplied from Rockwell. The host CPU uses the serial I/O port to transfer data to and from the modem IC.

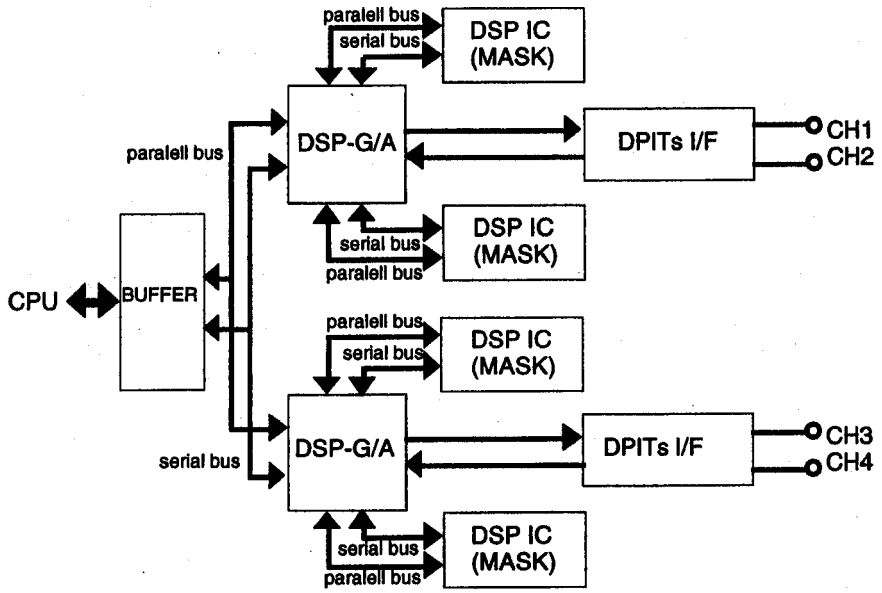
Using the parallel I/O port (2 bits) of the host CPU, the connection of the line channels with the modem can be switched. However, this switching is done on a slot by slot basis, and connection is made with the lowest channel number of the line modules installed in the expansion I/O slots. For instance, when the KX-TVS204 modules have been installed in three slots, CH1 (slot 1), CH5 (slot 2) or CH9 (slot 3) among the 12 channels is selected as the channel which can be connected to the modem.

RS-232C Interface Diagram



3. KX-TVS204 (4 PORT DPITs CARD)

DSP block is loaded with masked DSP (IC109) installed with a 1.3k word RAM.
This DSP interfaces and D-PITS line.
Each DSP disposes a digital voice region data for each channel described below. Mutual transformation, voice region digital data (64kBPS : 8bit/125us) and ADPCM data (32kBPS : 4 bit/125us), are executed. To detect a certain tone (for example DTMF tone or call progress tone) by analyzing input PCM data and to output a certain tone (for example DTMF tone or BEEP tone) as PCM data.
Timing Control on the DSP block is controlled by the system controller (IC101). System controller includes D-PITS interface, ADPCM compressed voice data transfer control between DSP and system memory, FIFO logic.
DSP receives commands from the host CPU through FIFO (IC101), then works based on the command.
This DSP execution program is stored in the internal ROM.
The D-PITS interface logic works to input and output the information data (D channel data) received and sent with the PBX through D-PITS with a HDLC controller (IC303) on a CPU block. It distributes voice region data (B1,B2 channel data) received and sent by the PBX through a D-PITS to each DSP(IC109A, IC109B).
The Parallel I/O port is controlled by the CPU.
The D-PITS transceiver includes the transceiver by transistor (Q261/Q262) and receiver by converter (IC261) and interfaces with PBX through the Pulse Trans (T291).
The 4DPITs card with 4 ports is optionally mounted on the KX-TVS200 for DPITs interfacing only. It shares the circuit board outline with the existing DSP card of the KX-TVS102. This enables the TVS200 to share its slot cabinet with the KX-TVS100. Along with the single circuit board design, DSPIC masking and the creation of six circuit board layers have been implemented. The general configuration is shown in the illustration below.



The KX-TVS204 has a construction in which the existing KX-TVS102 DPITs interface sections are connected through a dual buffer system. Two DSP gate arrays and four mask DSP ICs are mounted as a result. Two ports are provided, and by using only high/low lines, DPITs communication for two channels is enabled using a single port, and communication for 4 channels is enabled using two ports.
The host CPU must identify the previously mentioned slot addresses and card identification addresses for the KX-TVS204.

Table 3-3. SPECIFICATIONS OF THE DSP CARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
HOST I/F	50-pin Connector	Signals ×38, +5V ×2, -5V ×2, GND ×8
COL I/F	30-pin Connector	
DSP LSI (IC109 A ~ D)	Internal RAM	Running frequency : 57.344MHz (14.336MIPS)
	Internal ROM	1312 word ×16 (for Program/Data memory)
	Serial Port	20kword ×16 (not used)
	CODEC I/F	using D-PITS digital voice data in/out
		using SLT analog voice data in/out
SLAVE CONTROLLER (IC101)	FIFO	To communicate between Host CPU and DSP
	Parallel I/O Port	bit IA-3 : not used
		IA-2 : CPU-A detect when 0
		IA-1 : not used
		IA-0 : BELL-A detect when 0
		OA-1 : not used
		OA-0 : HOOK-A control (0: off-hook)
		IB-3 : not used
		IB-2 : CPU-B detect when 0
		IB-1 : not used
		IB-0 : BELL-B detect when 0
		OB-1 : not used
		OB-0 : HOOK-B control (0: off-hook)
		OX-3 : not used
		OX-2 : not used
		OX-1 : loop test enable when 0
		OX-0 : not used
	Serial Voice Port	for ADPCM Voice Data Transfer Control between DSP and System Memory
	D-PITS interface	D-PITS Frame Formatter and Transceiver

Table 3-4 SPECIFICATIONS OF THE KX–TVS204

BLOCK	SPECIFICATIONS	NOTE
HOST I/F Connector	50pin Connector	Signals X 38, -5V X 2,+5V X 2,GND
DPIT I/F	4pin Moduler	Port A : A ch,B ch DPITS I/F Port B : C ch,D ch DPITS I/F
DSP X 4	PSVI8C060BPJ	Running Frequency : 57.344MHz (14.336MIPS)
	Internal RAM	1312word X 16(for program / Data memory)
	Internal ROM	20kword X 16(only program memory)
	Serial I/O	D-PITS PCM voice data in/out
	Pararell I/O	B port : not use D port : Transfers data
	SD-CODEC Port	not use
	3 channels ADC	not use
DSP ext ROM	32Kword X 16bit	not use by using masked DSPIC
DATA FIFO	4byte/channel	To communicate between Host CPU and DSP
Pararell I/O	Total 20bit	bit IA-3: Card Identity(always 1) bit IA-2: not use(detect 1) bit IA-1: not use(always 1) bit IA-0: not use(detect 1)
	IA/IB : Readable both DSP & Host	bit OA-1: not use bit OA-0: not use
	OA/OB : Writeable only HOST	bit IB-3: Card Identity(always 1) bit IB-2: not use(detect 1) bit IB-1: not use(always 1) bit IB-0: not use(detect 1)
	IX/OX : Accessable only HOST	bit OB-1: not use bit OB-0: not use
		bit IX-3: Card Identity bits3(0) bit IX-2: Card Identity bits2(0) bit IX-1: Card Identity bits1(0) bit IX-0: Card Identity bits0(0)
		bit OX-3: not use (initialize to 1) bit OX-2: not use (initialize to 1) bit OX-1: not use (initialize to 1) bit OX-0: not use (initialize to 1)
TIME Slot Generator	Voice Channels Local Time Switch	Serial Voice Channel Configuration Regs. To Configure-Channel Number Assin -Source Select
PITS-I/F	PITS Data Buffer	DPITS Data Trancever Channel X 1
DMA-Channel	DMA Controller	DMA Channels for Voice Data Transfer
DPITS-I/F	4pin Moduler X 2	Ch A H-L:Ch1,Ch2 Dpits Data Line Ch B H-L:Ch3,Ch4 Dpits Data Line
	ON-HOOK Condition	Always linking to PBX ext port
	OFF-HOOK Condition	Always linking to PBX ext port
	BELL Detect	recive data from PBX
	DTMF Detect	recive data from PBX
	Tone Detect	recive data from PBX

4. KX-TVS102 (DPS/COL CARD)

Refer to the Service Manual for KX-TVS100

5. HARD DISK DRIVE

VPS uses a 3.5" intelligent magnetic disk device as an accumulator of voice data and storage of system program.

5 - 1. Drive Capacity

Formatted Capacity:

- ST31276A : 1276MB

*1MB = 1×10^6 bytes

5 - 2. Physical Configuration

Specification	ST31276A
Disk Type	Sputtered Thin Film
Head Type	Thin Film
Actuator Type	Rotary Voice Coil
Number of Disks	2
Data Surfaces	4
Data Heads	4
Servo	Embedded
Tracks per Surface	4893
Buffer Size	64KB
Track Density	4973tpi
Formatted Track Capacity	43,520-84,992bytes
Bytes per Block	512
Blocks per Drive	2,114,180
Sectors per Track (User)	85-166
Translate	Universal

5 - 3. Specification Table

Drive specification		
Manufacturer	Seagate	Seagate
Product name	Medalist 850xe	Medalist 1276
Guaranteed Mbytes	850	1,275
Guaranteed Sectots	1,661,184	2,501,856
Byte Per Sector	512	512
Default sectors per track	63	63
Default Read/Write heads	16	16
Default cylinders	1,648	2,470
Physical read/write heads	4	4
Disks	2	2
Recording dencity (Kbits/inch)	70	88
Track density (tracks/inch)	4,300	4,973
Spindole speed (RPM)	3,811	4,500
Internal data transfer rate (Mbits/sec max)	23.1 to 42.3	33.6 to 67.2
I/O data transfer rate (Mbytes per set max)	16.6	16.6
ATA data trasfer modes supported	PI0 modes 0,1,2,3,4	PI0 modes 0,1,2,3,4
Cache buffer (Kbyte)	120	64
Hight (inches max)	1.00	1.00
Width (inches max)	4.02	4.02
Depth (inches max)	5.77	5.77
Typical Weight (lb typical)	1.3	1.3
Track-to-track seek time (msec typical)	5	3
Average seek time (msec typical)	14	12.5
Full-stroke seek time (msec max)	34	24
Average latency (msec)	7.87	6.67
Power-on to ready (sec typical)	7	10
Standby to ready (sec typical)	3	6
Spinup curremt (peak)	1.25amp. (+12V)	1.20amp. (+12V)
Shock, operating (Gs, 11ms half-sine wave)	10.00	5.00
Shock, non operation (Gs, same above)	75.0	75.0
Vibration (Gs max at 22-400Hz non-recoverable errors)	1.0 (op.) 8.0 (non-op.)	0.5 (op.) 4.0 (non-op.)
MTBF	300,000	300,000
CSS cycles	40,000	40,000
Service life(years)	5	5

The specifications of the hard disk drive are subject to change without notice.

6. POWER SUPPLY

Power Card generates three kinds DC voltages (+5 V/-5 V, +12V), then supplies to the system.
Inside the main power supply, there is a voltage maintain circuit with big capacitor. That's why DC voltage is supplied steadly, in spite of AC voltage going lower temporary. The maximum DC voltage supply period by this capacitor is 300msec.
This power source asserts DC alarm signal, when +5V DC voltage goes lower than a certain threshold level. This signal is connected to Parallel Port inside IC301 through connector, Microprocessor can always check falling DC voltage. Power save disposition is executed when DC alarm signal assertion from power source is detected.

Table 3-5. SPECIFICATIONS OF THE POWER SUPPLY

Characteristic	Item	Specification
Input characteristics	AC input voltage	AC 97 to 276V (multiple) 110 to 120V ±15%, 220 to 240V ±15%
	Frequency	47 to 63 Hz
	Power consumption	55 W
	Leakage current	Less than 3 mA (division reference)
	Inrush current	Less than 40A
	Efficiency	60% (typ.)
Noise connector voltage and noise electrical field intensity		FCC Part 15, Subject J Class B
		Harmonic distortion supported
Output characteristics	+5V	
	Allowable deviation (overall fluctuation rate)	±0.25V
	Maximum	6.0A
	Minimum	0.1A
	Ripple voltage	Less than 200 mVp-p
	Ripple noise	Less than 300 mVp-p
	Overcurrent protection	Short-circuiting protection; reset by releasing the short-circuit
	Variable output range	4.6 to 5.6V
	Overvoltage protection	Output voltage cut off after detection of overvoltage; reset by turning AC power back on
	-5V	
	Allowable deviation (overall fluctuation rate)	±0.25V
	Maximum	0.5A
	Minimum	0.01A
	Ripple voltage	Less than 250 mVp-p
	Ripple noise	Less than 300 mVp-p
	Overcurrent protection	Short-circuiting protection; reset by releasing the short-circuit
	Variable output range	Fixed
	Overvoltage protection	None
	+12V	
	Allowable deviation (overall fluctuation rate)	±0.8V
	Maximum	0.5A (3.0A instantaneous maximum)
	Minimum	0.01A
	Ripple voltage	Less than 100 mVp-p
	Ripple noise	Less than 200 mVp-p
	Overcurrent protection	Short-circuiting protection; reset by releasing the short-circuit
	Variable output range	Fixed
	Overvoltage protection	None

CIRCUIT OPERATIONS

1. CPU CARD

1-1. System Reset (IC310)

When the power is on, the System Reset IC (IC310) initializes the whole system. MRSTN, output from IC310, is input to the RSIN (119 pin) of IC302. During RSIN's low period, IC302 is self-initialized and drives LRSTN (49 pin) and HLTN (50 pin) to low order to make the external device initialize.

LRSTN is distributed as shown below. LRSTN should be driven in High level normally. Only when the power is on, it is asserted in Low.

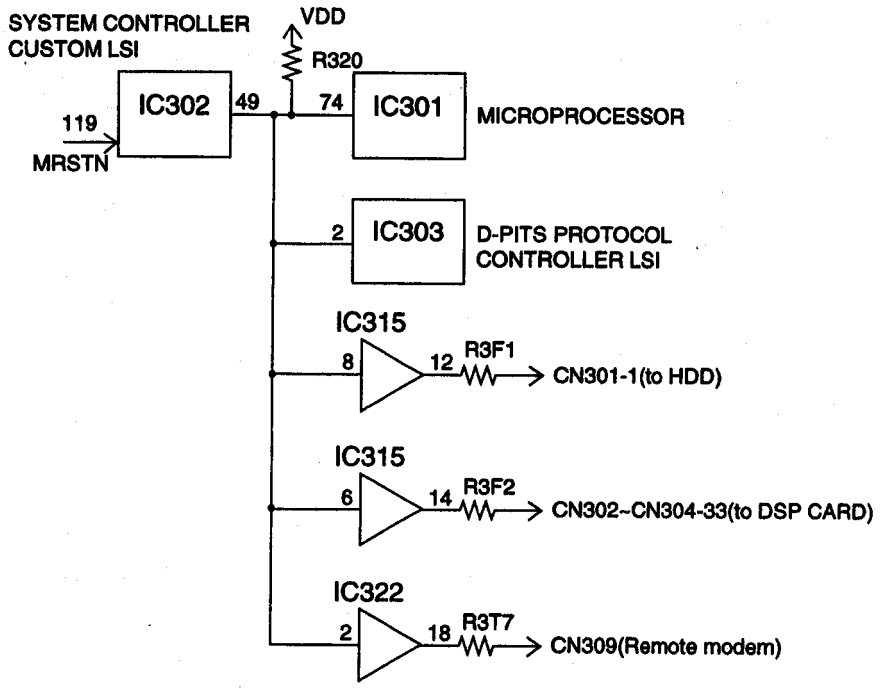
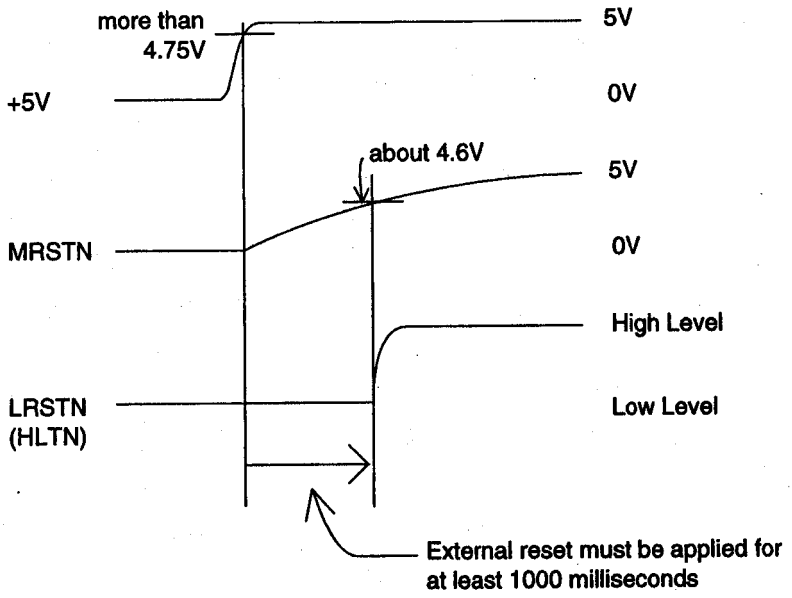


Fig. 4-2. System Reset Distribution



Timing 4-1. System Reset

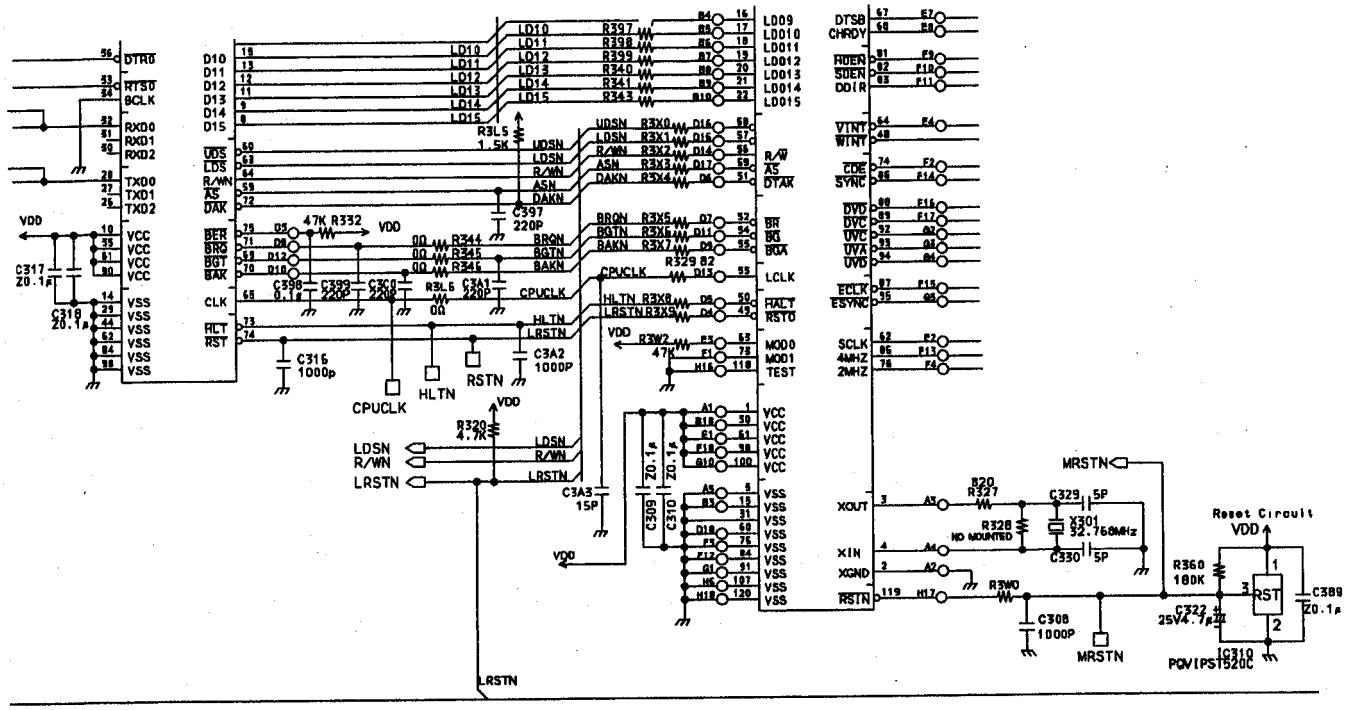


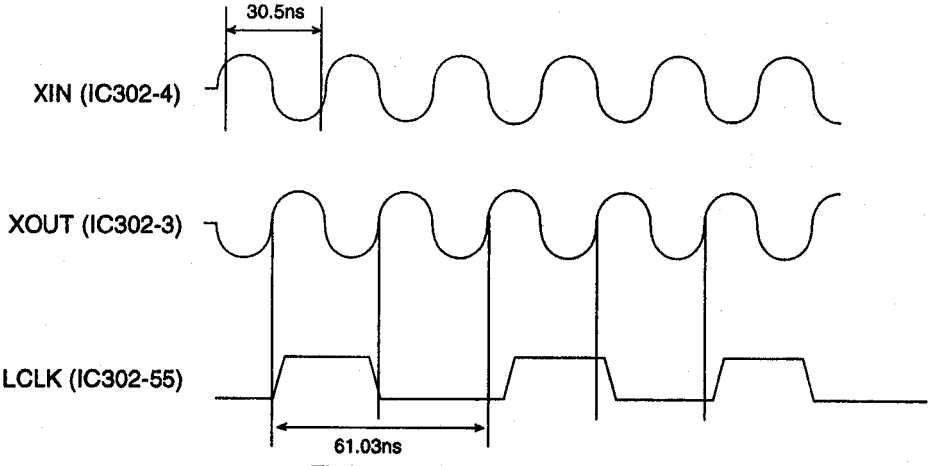
Fig. 4-1. System Reset Signal Flow

1-2. Microprocessor Interface (IC301, IC302)

System controller (IC302) controls the Microprocessor (IC301) to access external resources (i.e. Memory, I/O device).

(1) Processor Clock

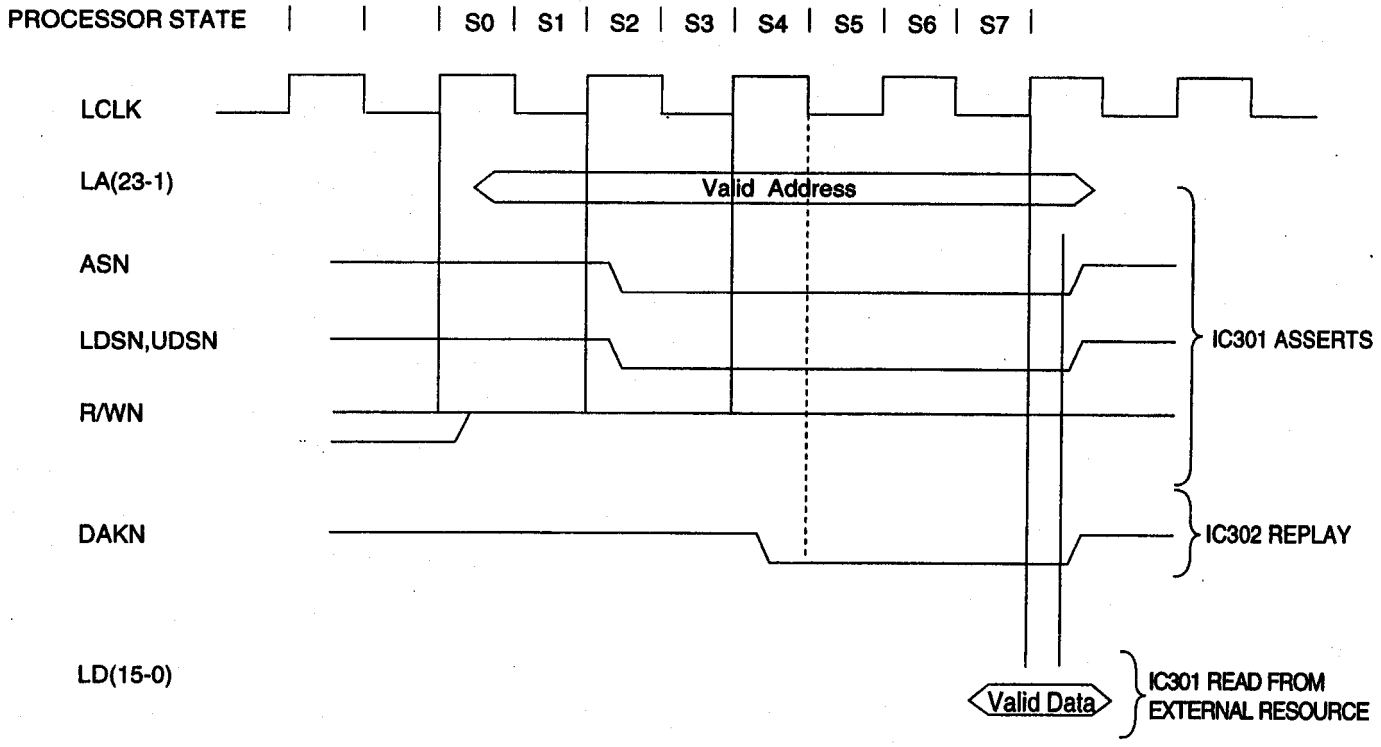
IC302 provides a processor clock from the LCLK (55) pin. Output of X'tal connected to IC302 is output from the LCLK pin divided in half inside the IC302.



Timing 4-2. Processor Clock

(2) Read Cycle

In the read cycle IC301 outputs a valid address to A(23-1) in S0 state. Then in S2 state, IC301 asserts a signal line of ASN(59), UDSN(60), LDSN(63) and R/WM(64). IC302 decodes the condition of these signal lines and replies to DAKN(IC302-5 pin) in needed timing (normally in S4 state). By DAKN's reply, IC301 reads the valid data on the LD(15-0) line. (Refer to Timing 4-2).



Timing 4-3. Read Cycle

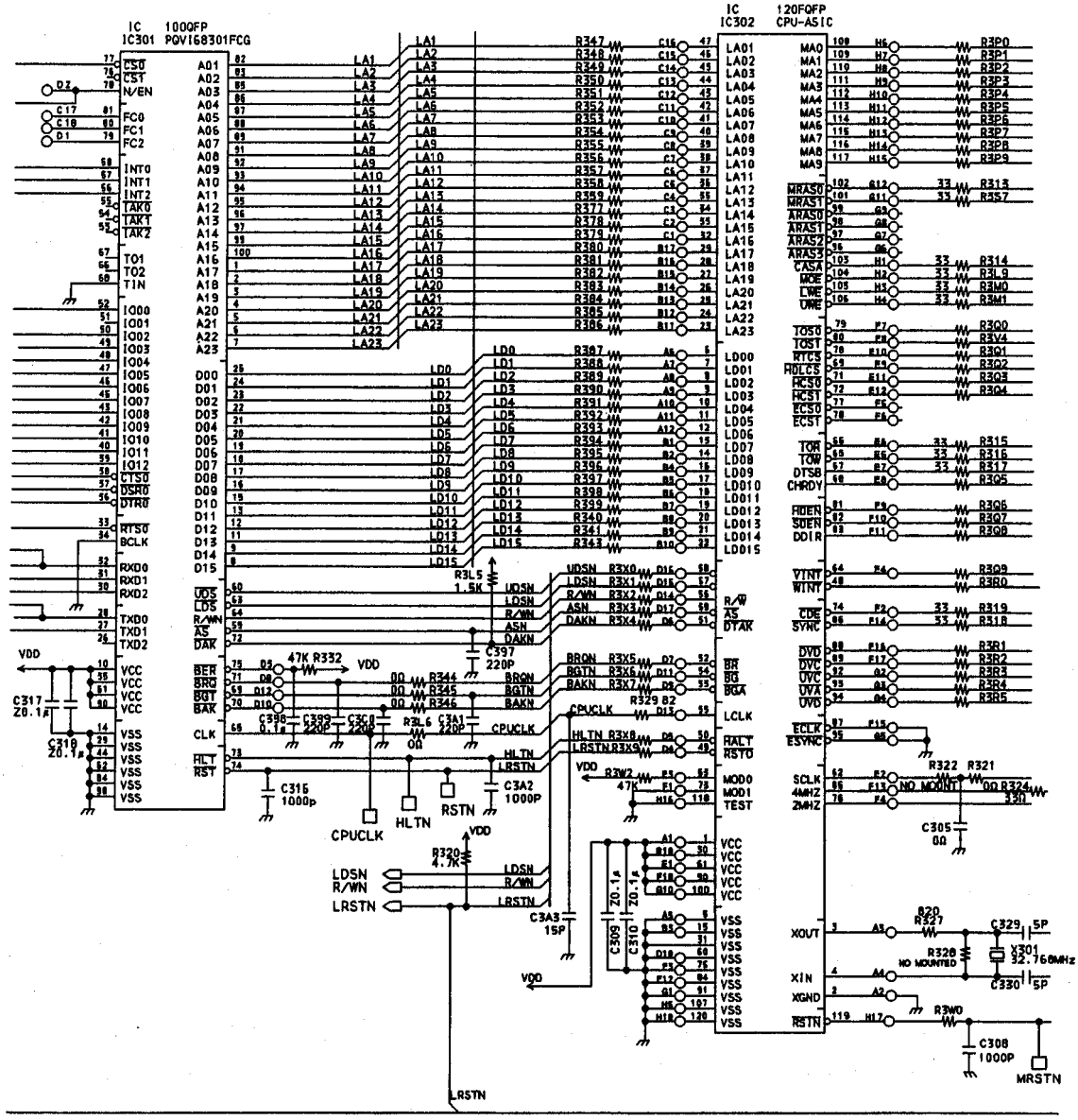
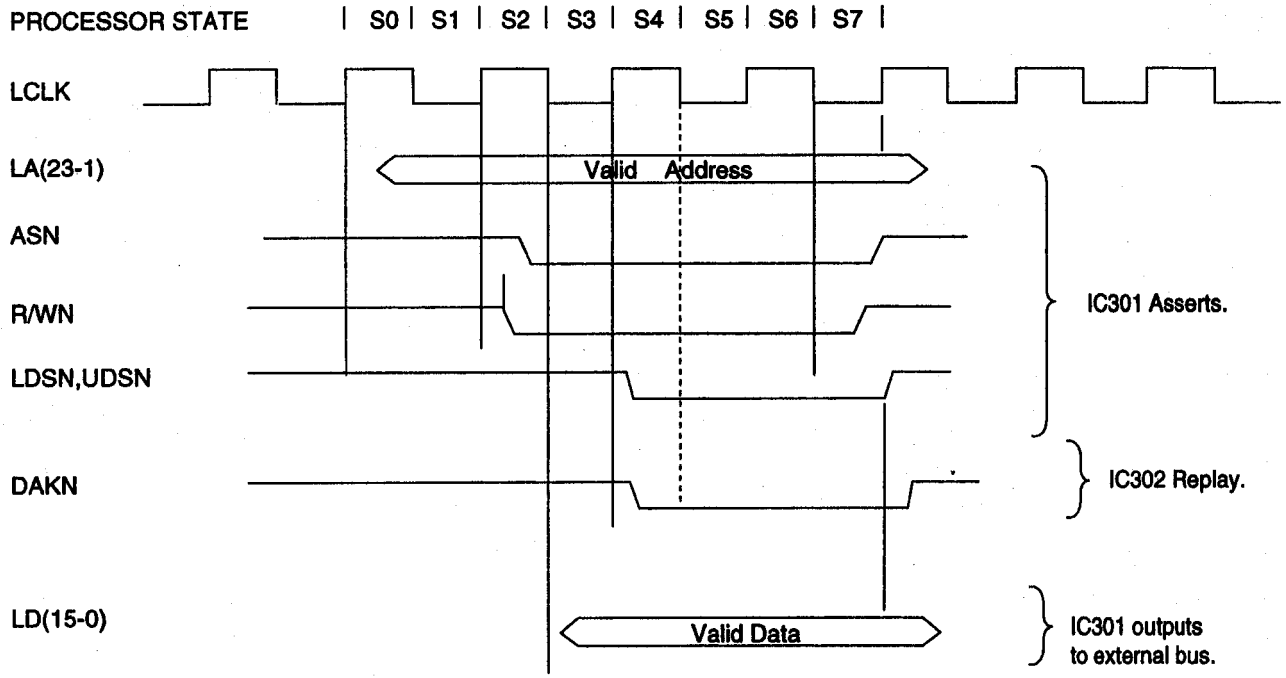


Fig. 4-3. Microprocessor Interface

(3) Write Cycle

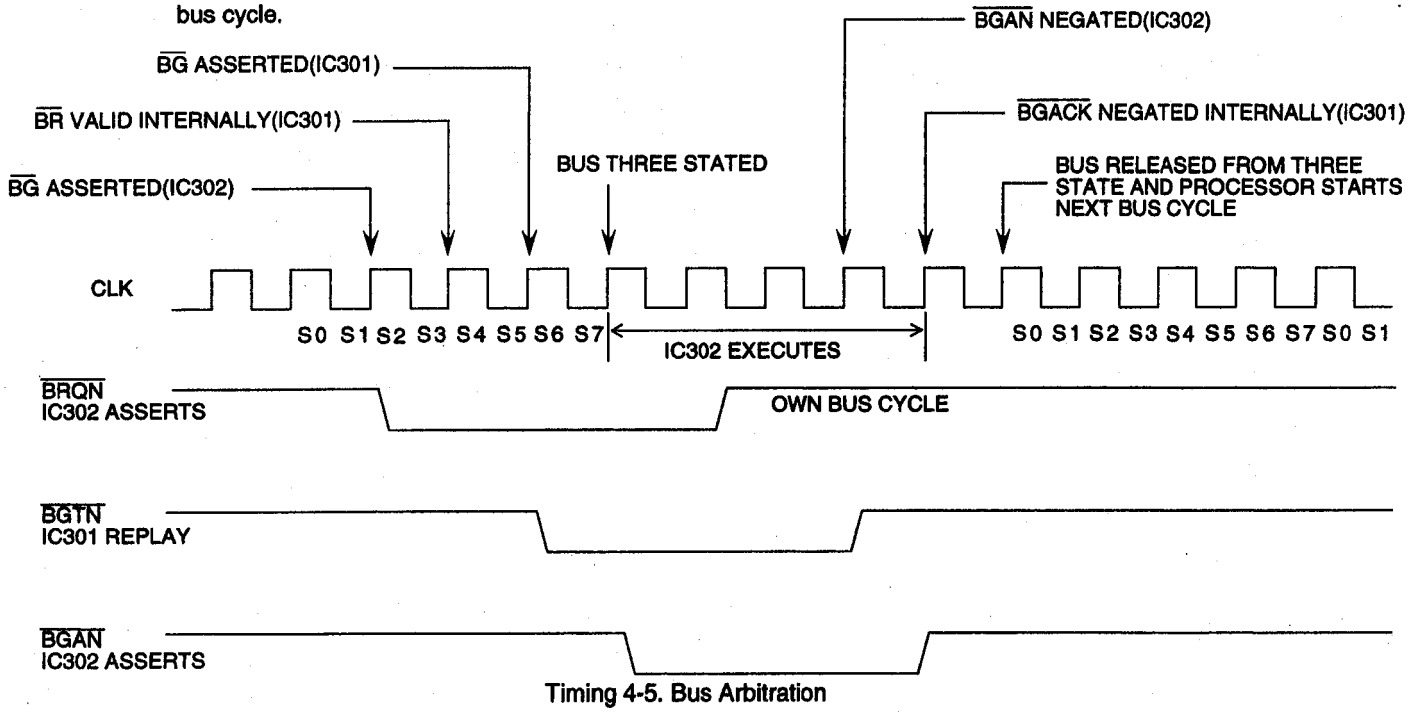
In write cycle IC301 outputs valid address to A(23-1) in S0 state. Then in S2 state, IC301 asserts a signal line ASN(59), R/WN(64). In S3 state, it outputs valid data to LD (15-0). In S4 state it asserts the signal line of UDSN(60) and LDSN (63). IC302 decodes the condition of these signal lines and replies to DAKN(IC302 - 51pin) in needed timing (normally in S4 state). IC302 terminates write cycle by the reply of DAKN. An External resource is controlled to take in effective data on LD(15-0) by a control signal generated from the system controller.



Timing 4-4. Write Cycle

(4) Bus Arbitration Cycle

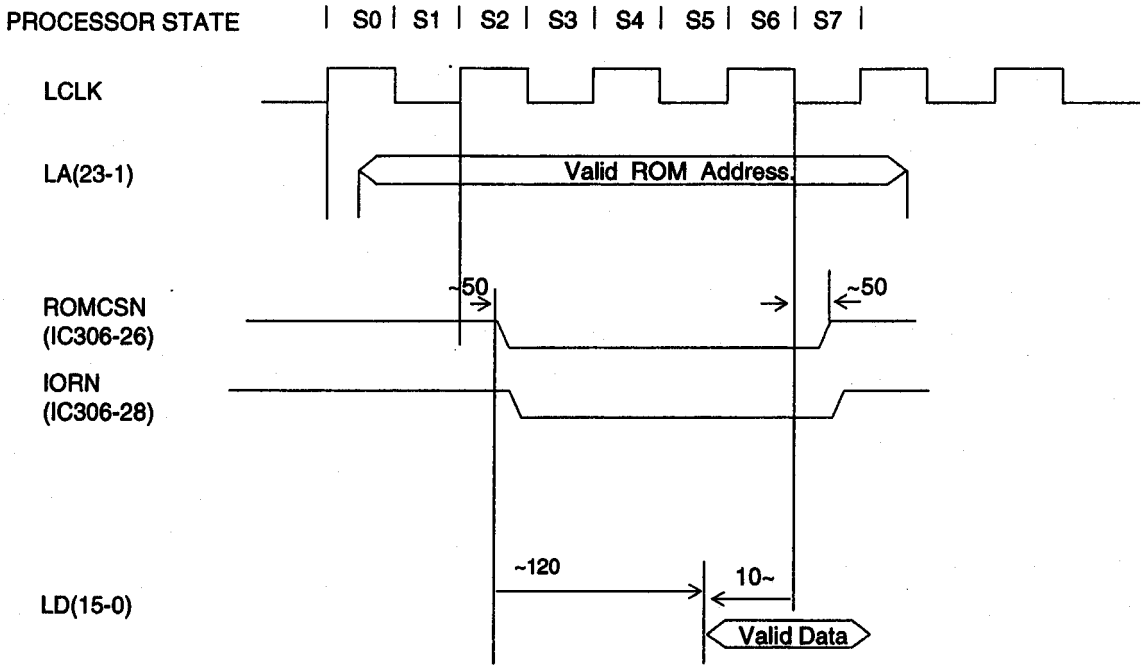
The system controller (IC302) itself should access to system memory (i.e. transfer to system memory of ADPCM Data, execution of DRAM refresh). System controller (IC302) requires the Microprocessor (IC301) to hand over bus ownership with asserting BRQN (IC302-52 pin). When IC301 finishes its own bus cycle, it replies to BGTN(IC301 - 69) and hands over bus ownership to IC302. After detecting assertion of BGTN, IC302 asserts BAKN (IC302 - 53) then executes access to system memory for itself. At that time IC302 negates BRQN. After terminating the access to system memory, IC302 negates BGAN to hand over Bus ownership to the Microprocessor (IC301). After detecting negation of BGAM, IC301 starts executing its own bus cycle.



Timing 4-5. Bus Arbitration

1-3. System ROM (IC306)

System ROM has a program to initialize the system, diagnose itself and a loading program to load the application program from HDD to System RAM. Right after System Reset is negated, the Microprocessor (IC301) always reads the program execution address stored in the address "00000h" of System ROM. Based on that execution address information, IC301 starts to execute program initializing inside the system of ROM.



Timing 4-6. System ROM Read

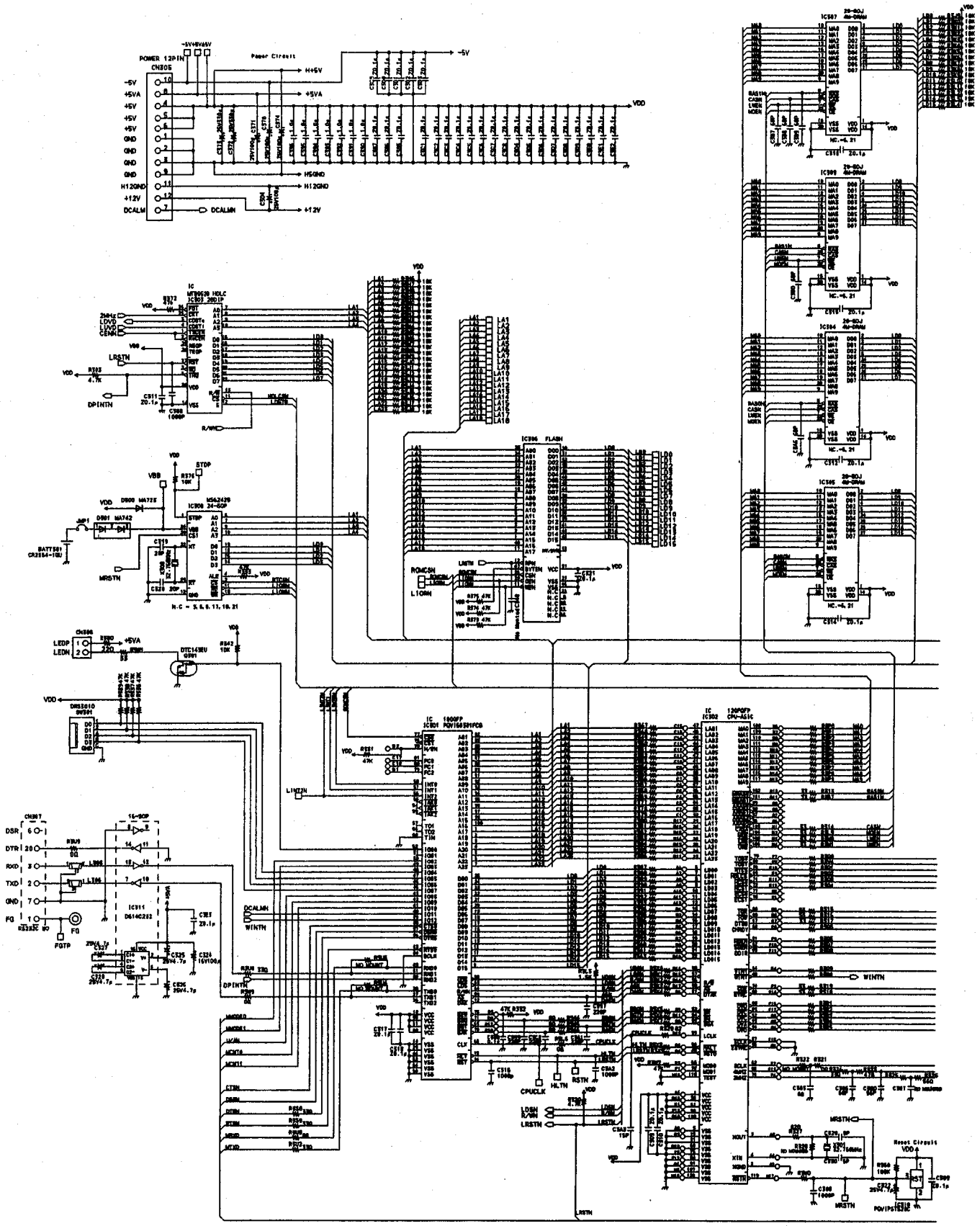


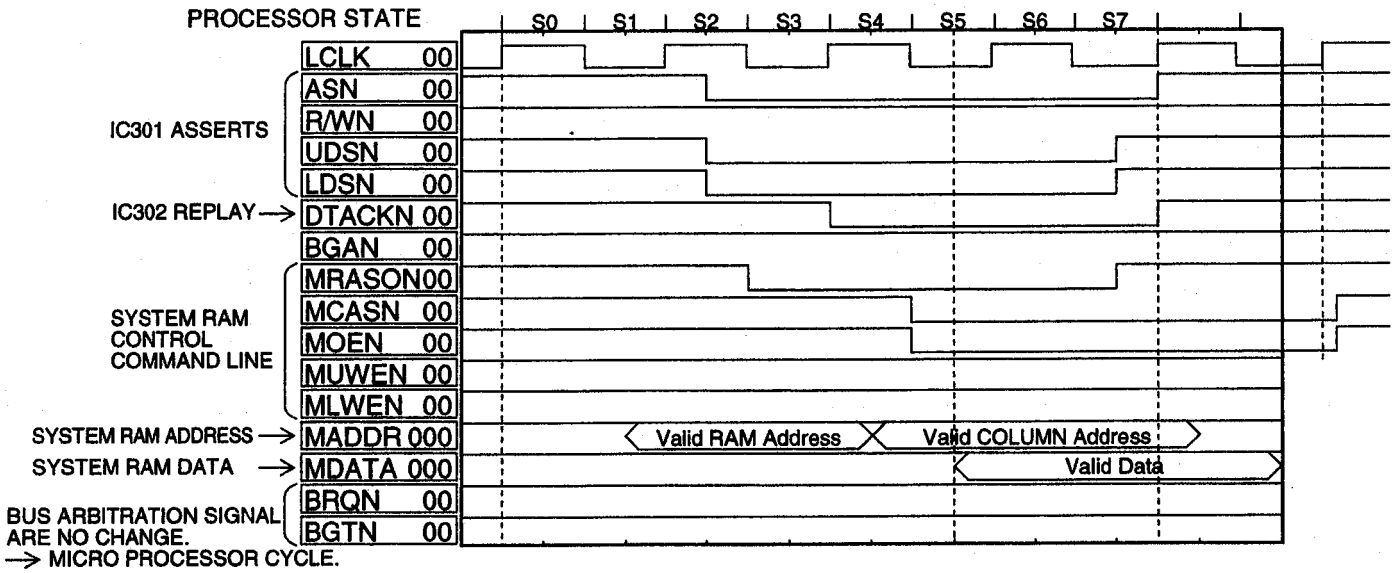
Fig. 4-4. System ROM Read

1-4. System RAM (IC304, 305, 307, 309)

An Application program is loaded to system RAM by a ROM based Program. The execution program will then run on the system RAM. System RAM uses a 4M bit Dynamic RAM . This access timing is controlled by the system controller (IC302). The operations of IC304 and IC305 are described here.The operations of IC307 and IC309 are exactly the same as those of IC304 and IC305 except that the timing of the RASIN select signal differs.

(1) System RAM Read Cycle by Microprocessor

Microprocessor executes a normal read cycle in the system RAM's Read cycle by a IC301 (Microprocessor). IC302 (System controller) decodes the condition, then generates the dynamic RAM's read signal.



Timing 4-7. System RAM Read Cycle by Microprocessor

In read cycle MRASON(IC302 - 102, memory RAM address strobe) is asserted in low in the falling edge of the S2 state. IC303 and IC304 take address information on MA(9-0) in MRASON falling edge. Next MA(9-0) changes in S4 state. CASN(IC302 - 103) (Column Address Strobe) and MOEN (IC302-104) (Memory Output Enable) are asserted in low in S4 stat's falling edge. IC304 and IC305 take address information on MA(9-0) in CASN's falling edge. They output their own data to LD(15-0) because MOEN is asserted.
The Microprocessor takes effective data on LD(15-0) in S6 state falling edge.

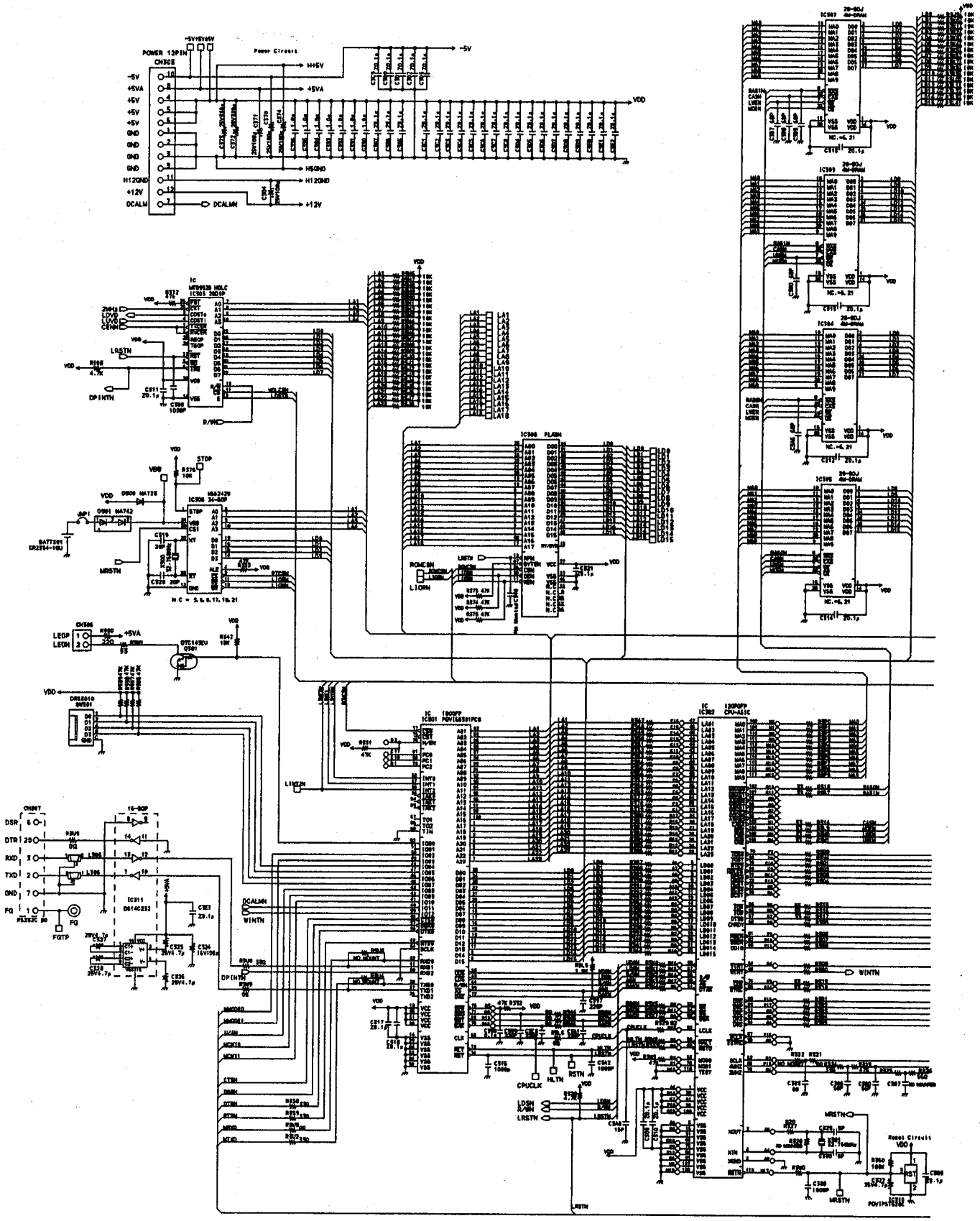
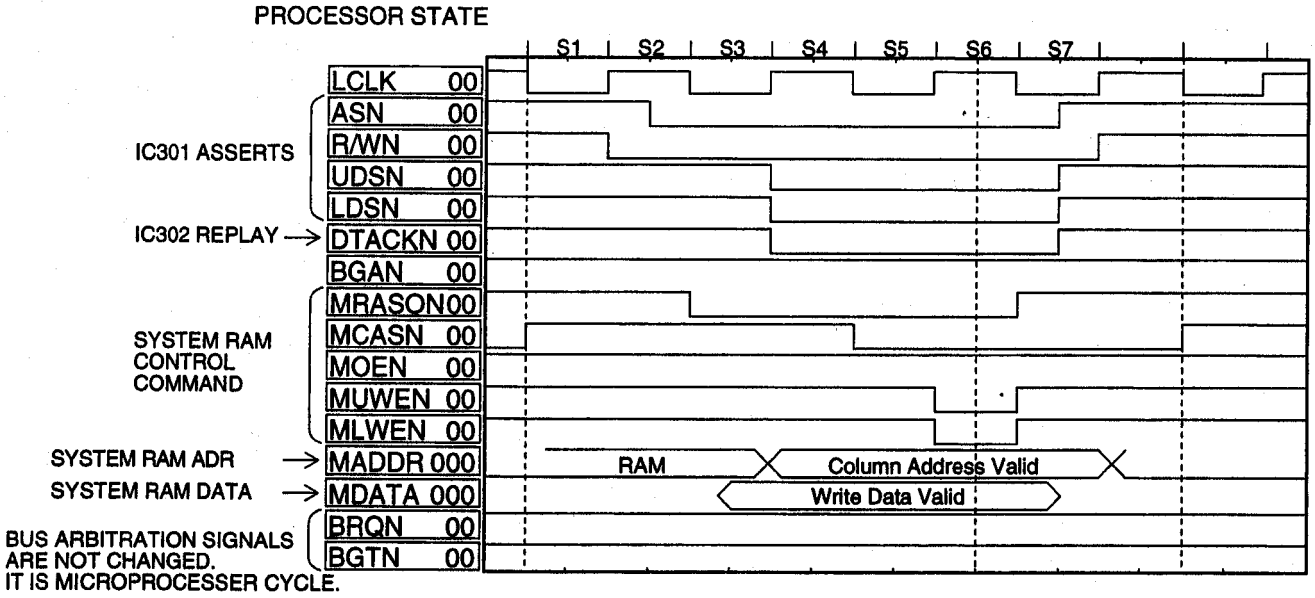


Fig. 4-5. System RAM

(2) System RAM Write Cycle by Microprocessor



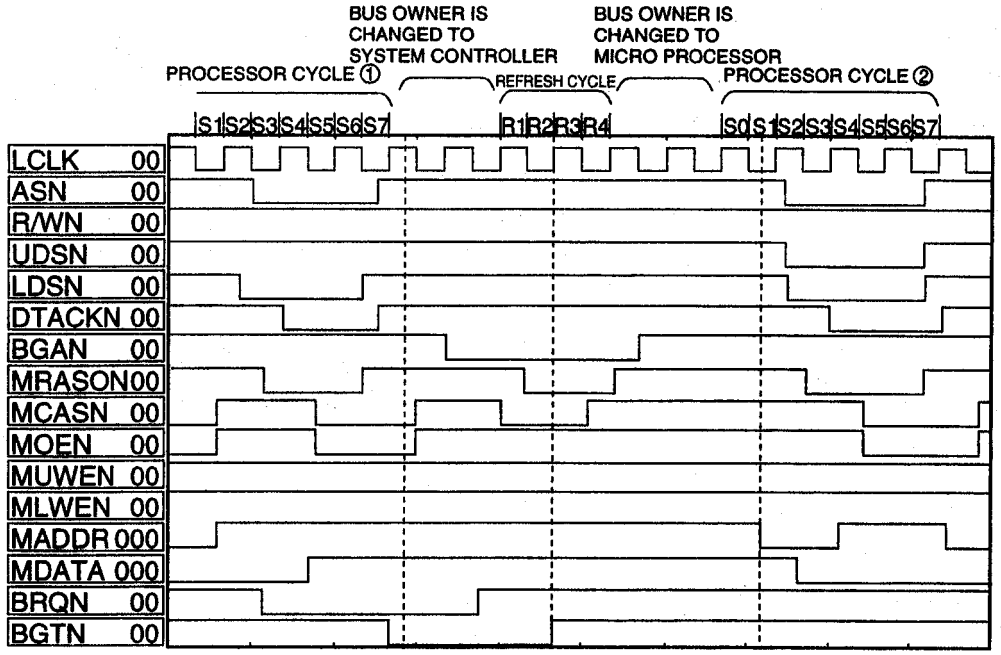
Timing 4-8. System RAM Write Cycle by Microprocessor

In System RAM Write Cycle by Microprocessor, MRASON (IC302-102) = Memory RAM Address Strobe, is asserted in low in the falling edge of the S2 state. IC303 and IC304 take address information on MA(9 - 0) in the falling edge of MARASON. MA(9 - 0) varies in S4 state. CASN (Column Address Strobe) is asserted in the falling edge of S4 state. IC303 and IC304 take address information on MA(9 - 0) in the falling edge of CASN. IC301 outputs the effective data to LD(15 - 0), the period from S3 state to S6 state. IC302 asserts UWEN (106) = Upper memory write enable and LWEN (105) = Lower Memory Write Enable, in S6 state. IC303 and IC304 take the data on LD(15-0) in the falling edge of UWEN and LWEN into the inside of memory.

(3) Refresh Cycle by System Controller

In order to preserve the internal data of the Dynamic RAM used as System Memory, System Controller (IC302) executes a bus cycle, called Refresh cycle, every 16μs. In order to execute the Refresh Cycle, System Controller demands Bus Ownership from Microprocessor (IC301) . After receiving bus ownership from the Microprocessor, System Controller executes Refresh cycle. After the Refresh cycle is completed, System Controller hands over Bus Owner ship to the Microprocessor. (Refer to 1-2. (4) Bus Arbitration Cycle). The Refresh cycle executed is called "CAS BEFORE RAS Refresh". In case of not being executed periodically, the Refresh cycle is hold in the Dynamic RAM. The Data is purged.

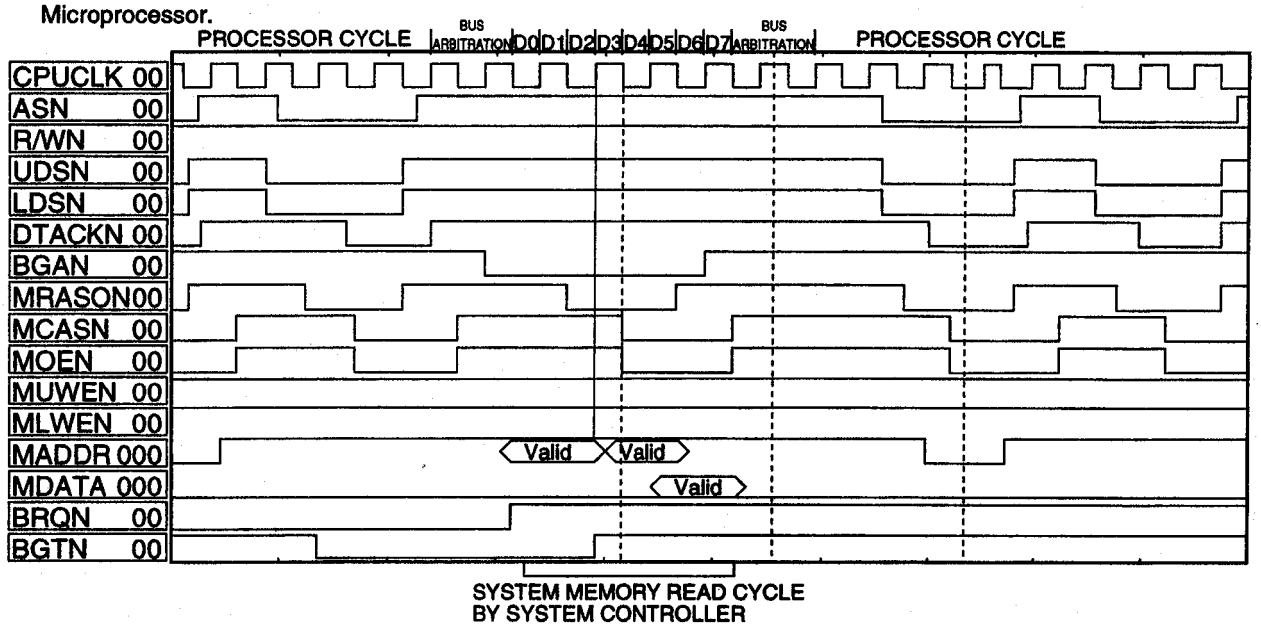
The Refresh cycle is executed while BGAN (IC302 - 53) is asserted, namely system controller is in the period of Bus Ownership. This cycle starts from LCLK (IC302 - 55)' s rising edge after the BGAN is asserted, then is completed during 2xLCLK. CASN (IC302 - 103) is asserted in the rising edge of R1 state. Each of them is negated in the falling edge of R3 state and in the rising edge of R4 state. Around Refresh Cycle Arbitration cycle is executed.



Timing 4-9. Refresh Cycle by System Controller

(4) System RAM Read Cycle by System Controller

In time Message Delivery to the extension line, the DSP Card requires System Controller (IC302) to send the ADPCM Data on System memory. System controller, accepting this requirement, demands Bus Ownership from the Microprocessor (IC301). Once System controller receives Bus Ownership from the Microprocessor, the System RAM read cycle is executed. After that System Controller hands over Bus Ownership to the Microprocessor.



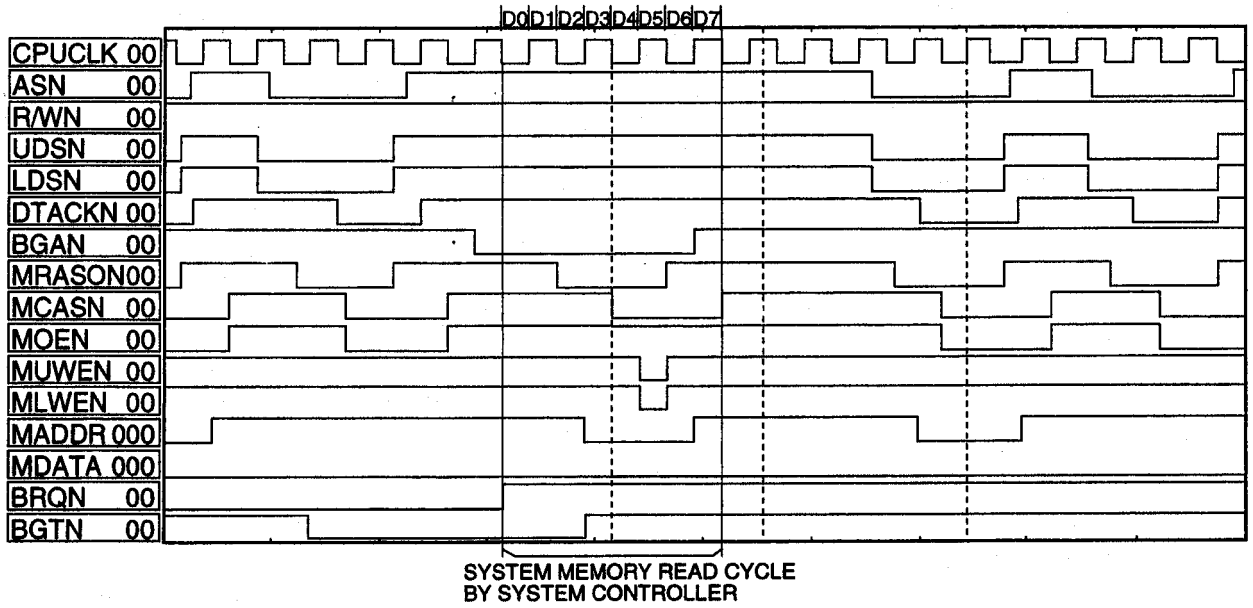
Timing 4-10. System RAM Read Cycle by System Controller

Once System Controller rewires Bus Ownership from the Microprocessor, it asserts BGAN (IC302 - 53) in low and executes the System - Memory Read cycle. This read cycle starts from CPUCLK's rising/falling edge after BGAN is asserted and ends during 4xCPUCLK.

The System Controller outputs a destination address to MA(9 - 0) in D0 state. MRASON is asserted in the leading edge of D2 state and MA (9 - 0) switches over in D3 state of the leading edge. MCASN and MOEN are asserted in the leading edge of D4 state. IC303 and IC304 start outputting the data to LD (15 - 0). System controller takes in the effective data on LD(15-0) in the leading edge of D7 state. (The data taken in is sent to the DSP Card through the extension bus. In order to return bus ownership to the Microprocessor, System controller negates BGAN in the leading edge of D7 state.

(5) System RAM Write Cycle by System Controller

In time Message receiving from the extension line, ADPCM data generated by the DSP is added to the system RAM address information of where to transfer the DSP card. Then ADPCM data is sent to the system controller. Receiving this information, System Controller requires the Microprocessor to hand over Bus ownership in order to write designated addresses. By this requirement, system controller obtained bus ownership executed by the System Ram Write cycle.



Timing. 4-11 System RAM Write Cycle by System Controller

In Write cycle by System Controller, the output timing of MRASON, MA(9 - 0) and MCASN are the same as the Read cycle. In Write cycle MOEN is not asserted , and MUWEN and MLWEN are asserted in D5 state. In time, BGAN is asserted in low, System Controller outputs effective data to LD (5 - 0). This effective data is stored in IC303 and IC304 at the falling edge of MUWEN and MLWEN .

1-5. System Port

The System Port Function is provided by PIO (Parallel Input Output Control) inside IC301.

System Port's functions are

- to control the Power Indicator (LED)'s ON/OFF
- to read the condition of the Rotary switch
- to read the condition of DCARM (DC Alarm) input from the Power Unit.

(1) Power Indicator (LED) ON/OFF control

The Power Indicator (LED)'s ON/OFF is controlled by a IC301 - pin 52. This pin is connected to the base of the digital transistor Q301. When IC301 - 52 is "High", between the emitter and collector of Q301, it becomes transmissible and LED turns on. When IC301 - 52 is "Low", between emitter and collector of Q301, it becomes non-transmissible and LED turns off.

(2) Rotary switch port

The Rotary switch is surrounded by IC301 - pin 45 ~ pin 48.

(3) DC ALARM PORT

When Power Card detects low DC voltage, it drives the CN 305 - 5 pin to low, then informs the CPU Card of the DC power condition. The input signal from CN305 - pin 5 is taken as DCALMN from the IC301-pin 40. This signal normally is "High".

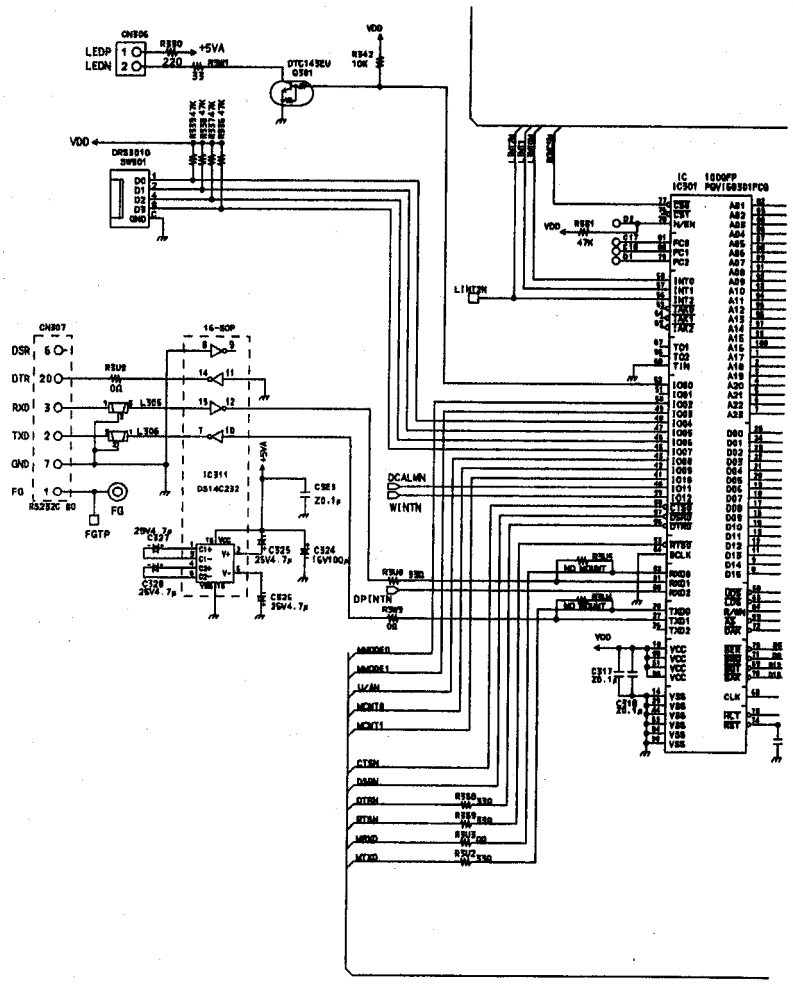


Fig. 4-6. System Port and RS-232C Interface

1-6. RS-232C Interface

The RS-232C interface is provided by SIO (Serial Input Output Controller) built-in the IC301.

(1) Data Format

When a data character to be transmitted is placed in the SIO, the serial interface automatically adds one start bit before the data bits (lower order bits are output first) and the specified number of stop bits after the data bits. When parity (even, odd) is specified in the mode register, a parity bit is inserted before the stop bit.

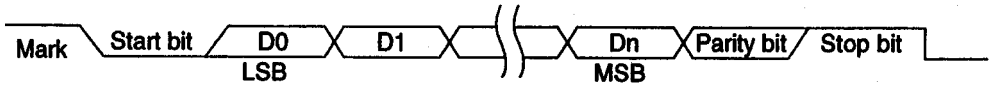


Fig. 4-7. Data Frame

(2) Data Transmission

The Microprocessor checks the DSR (IC301 - 37): Data Set Ready is low, i.e. terminal side's preparation for receiving data finishes, then starts transmission. After transmitting the start bit, the transmit controller automatically appends a parity bit and stop bit to the data character of the specified length and shifts these out to the TxD line. When the next data character has been written to the transmit data buffer, transmission continues with the start bit of the next data character following the stop bit of the current data.

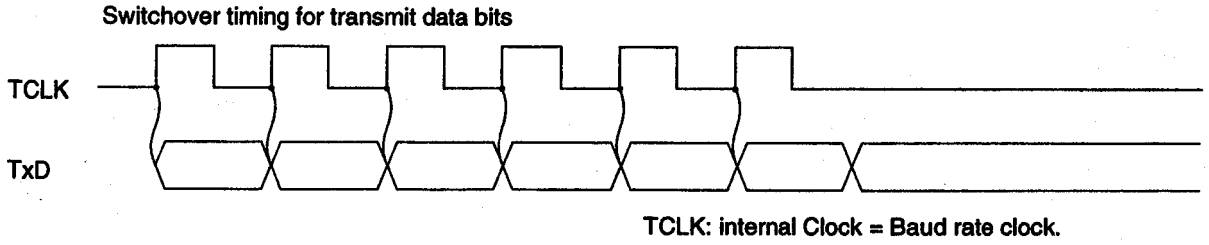


Fig. 4-8. Switchover Timing for Transmit Data Bits

(3) Data Reception

The RxD line is high when no data is in it (mark status). The beginning of a start bit is detected when the input goes low.

For receiving, the first low sampled RXD is detected and, if the sampled data are low for four internal CLKs, this low level is considered to be a valid start bit. The center point of the following data bits is then determined and each data bit is sampled on the TCLK falling edge.

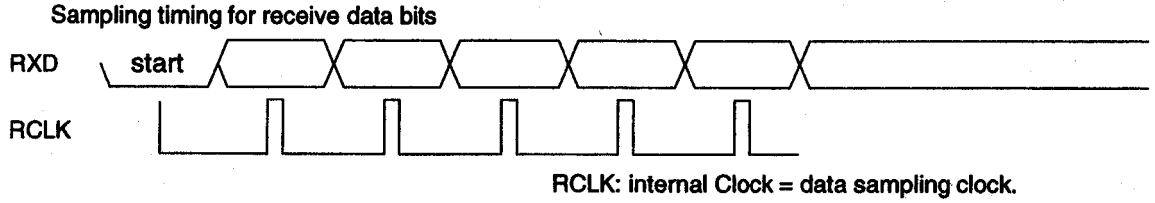


Fig. 4-9. Switchover Timing for Receive Data Bits

(4) RS-232C Tranceiver (IC311)

The IC311 is a transceiver IC only for RS-232C. IC311 possesses a built-in DC/DC Converter and generates ±10 V needed for the RS-232C interface. Each terminal voltage of the DC/DC converter block is in Figure 4-6.

1-7. Real Time Clock

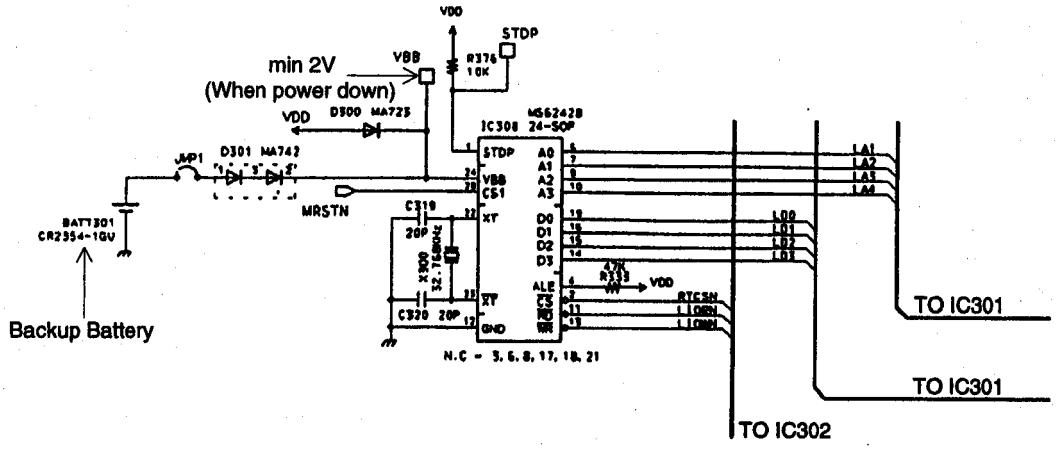
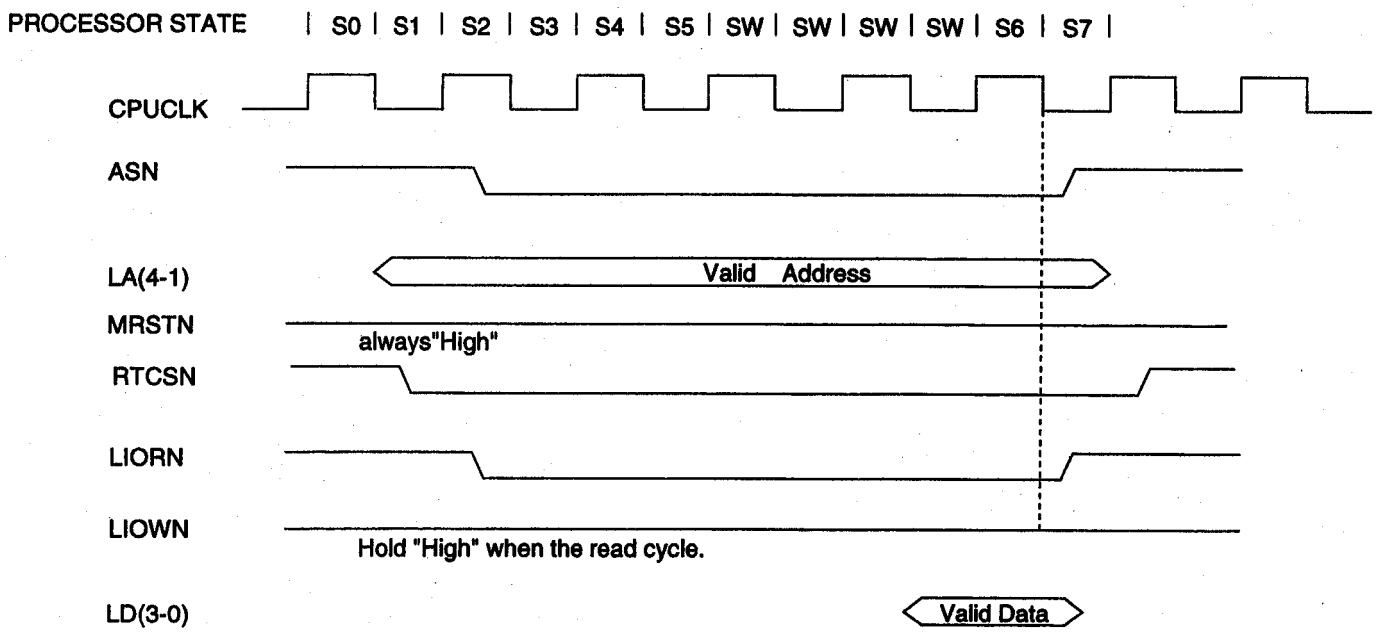


Fig. 4-10. Real Time Clock

The Real Time Clock is provided by IC308. IC308 is a Real Time Clock IC with a fail-safe calender to be able to read and write from seconds. To interface with the Microprocessor four data buses=(LD<3-0>), four address buses=(LA<4-1>), two control buses (LIORN, LIOWN) and two chip select (RTCSN, MRSTN) are needed for set the time/modification/read out.

(1) Microprocessor Read Cycle

Read timing of time data from IC308 by Microprocessor is shown in timing 4-12.

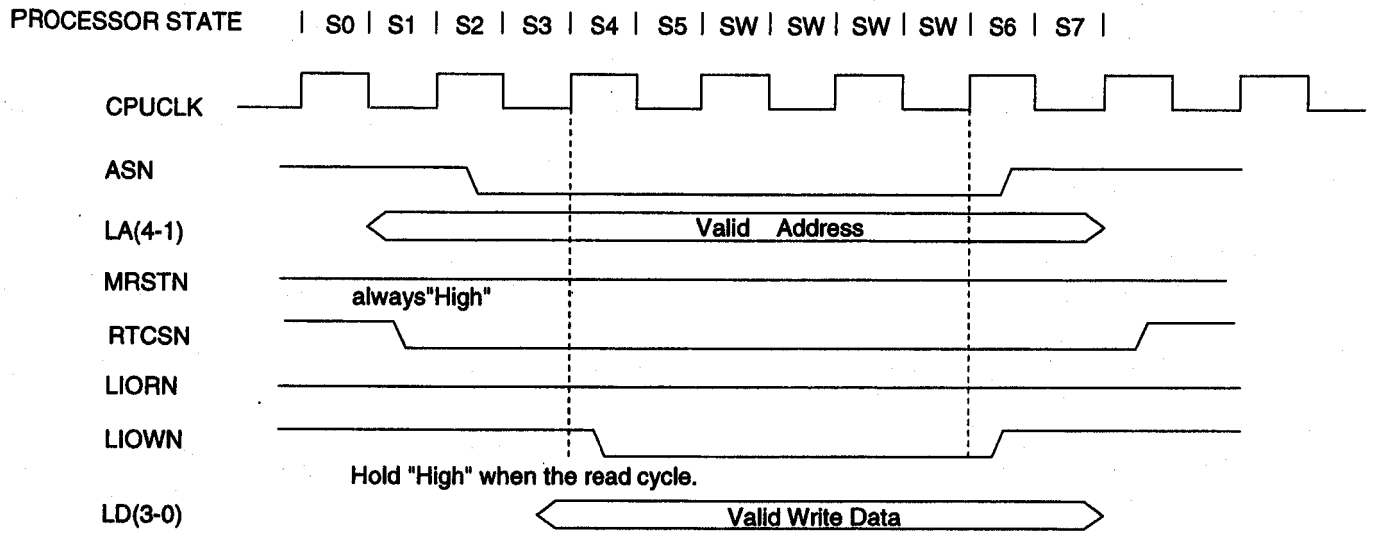


Timing 4-12. Real Time Clock Read by Microprocessor

The Microprocessor (IC301) outputs valid Address to LA(4-1) in S1 state. System Controller (IC302) asserts RTCSN in low. System Controller asserts LIORN to low in S2 state. To Respond to low assertion of LIORN, the IC308 outputs the internal register corresponding with LA(4 - 1). At that time to LD(3 - 0) the Microprocessor takes in effective data on LD(3 - 0) in the falling edge of S6 state.

(2) Microprocessor Write Cycle

Time data's wire timing to IC308 by Microprocessor is shown in Timing 4 - 13.



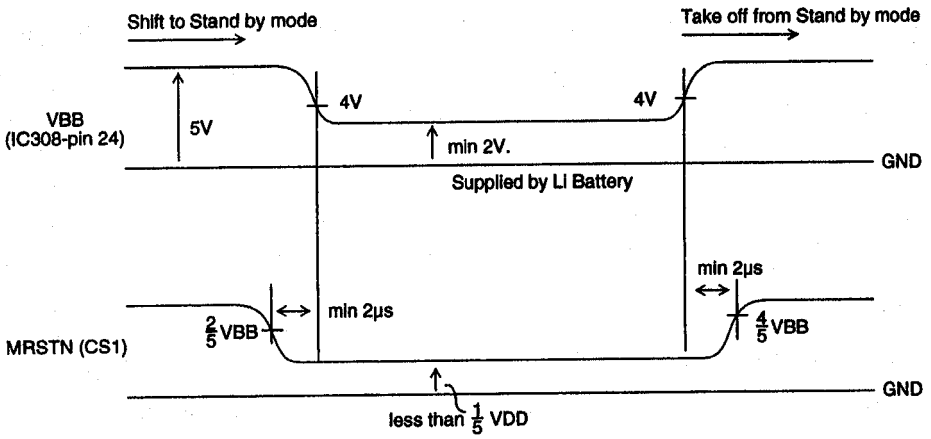
Timing 4-13. Real Time Clock Write Cycle by Microprocessor

The Microprocessor (IC301) outputs Valid Address to LA (4 - 1) in S1 State. System Controller (IC302) asserts RTCSN in low. The Microprocessor outputs Valid Write Data to LD (3 - 0) in S3 state. System Controller asserts in low in time from the rising edge of S4 state to the rising edge of S6 state. IC 308 takes the effective data on LD (3 - 0) in the rising edge of LIOWN.

(3) Battery Back Up Interface

IC308 has two modes: operation mode and standby mode. Operation mode is guaranteed the interface with Microprocessor and is the condition to be able to setting time/modification/read and write.

If provided more than 4/5 of VDD voltage is relayed to the CS1 terminal (pin 20), it becomes the operation mode. If less than 1/5 of VDD voltage is relayed to the CS1 terminal (pin 20), it becomes the stand-by mode. By IC308 checking time function inside IC works but the interface with Microprocessor is not guaranteed. In this mode the consumption of the current decreases. In order to switch over these two modes (operation mode and stand-by mode), The MRSTN signal is connected to the IC308 CS1 terminal.



Timing 4-14. Battery Backup

When Power goes down, MRSTN signal changes the level lower than 2/5 V_{BB} before V_{BB} reaches at 4V. When Power goes up, MRSTN signal changes the level higher than 4/5 VBB after V_{BB} reaches at 4V. With this MRSTN signal, a certain switch over (operation mode and stand-by mode) is guaranteed. In order to guarantee the checking time function of IC308 in stand-by mode, more than 2V voltage should be added to V_{BB}.

This guaranteed voltage is supplied by the lithium battery.

1-8. D-PITS Protocol Controller

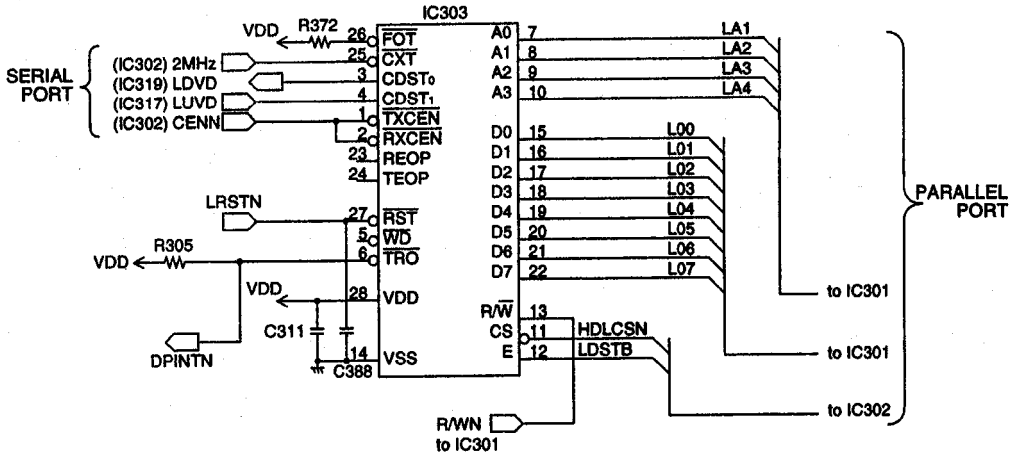


Fig. 4-11. D-PITS Protocol Controller Interface

When Panasonic KX-TD series PBX and VPS are connected, VPS adopts a Data Format and communication protocol based on X.25 (CCITT) level 2 in order to exchange its own status and command parties between the VPS and PBX mutually. This data communication is provided by IC303.

The DPITS Protocol Controller has two ports. The serial port transmits and receives formatted data packets and the parallel port provides a Microprocessor interface for access to various registers in the Protocol Controller.

The Microprocessor Port allows parallel data transfers betwen the Protocol Controller and a Microprocessor bus. This interface consists of Data Bus (LD7 - LD0), Address Bus (LA4 - LA1), Data Strobe (LDSTB), Chip Select (HDLCSN) and Read/Write Control (R/WN). The Microprocessor can read and write to various registers in the Protocol Controller. The DPINTN, active Low output indicates and interrupt requests to Micrprocessor. The interrupt request will be asserted when the packet data transmission is complete or four more packet data receptions are confirmed.

The serial port handles bit oriented protocol structure and formats the data as per the packet switching protocol defined in the X.25 (level 2) recommendations of the CCITT. It transmits and receives the packeted data (information or control) serially as shown in Figure 4-12.

FLAG	DATA FIELD	FCS	FLAG
1BYTE	N Byte (n ≦ 2)	2 Bytes	1 Byte

Fig. 4-12 D-PITS Data Packet Format

Flag:

The flag is a unique pattern of 8 bits (01111110) which defines the frame boundary. The transmit section generates the flags and automatically appends them to the frame to be transmitted. The receive section searches the incoming packets for flags on a bit-by-bit basis and establishes frame synchronization. The flags are used only to identify and synchronize the received frame.

Data:

The data field refers to the Address, Control and Information fields defined in the CCITT recommendations. A valid frame should have a data field of at least 16 bits.

Frame Check Sequence (FCS):

The 16 bits following the data field are the frame check sequence bits. The generator polynomial is:

$$G(x) = x16 + x12 + x5 + 1$$

The transmitter calculates the FCS on all bits of the data field and transmits after the data field and before the end flag. The receiver performs a similar computation on all bits of the received data and FCS fields. The result is compared with $FOB8_{Hex.}$ If it matches, the received data is assumed to be error free.

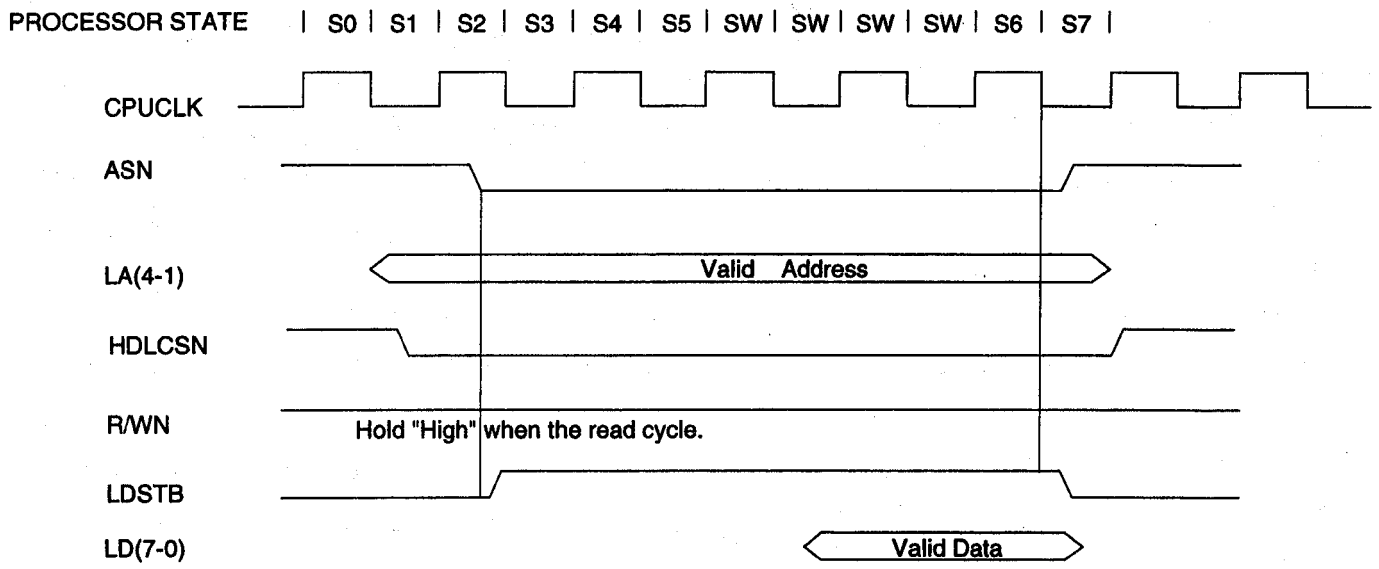
Zero Insertion and Deletion:

The Protocol Controller, while sending either data or the 16 bits FCS, checks the transmission on a bit-by-bit basis and inserts a ZERO after every sequence of five contiguous ONEs (including the last five bits of FCS). This ensures that the flag sequence is not simulated. Similarly, the receiver examines the incoming frame content and discards any ZERO directly following the five continuous ONEs.

In the serial port, the formatted data packets are shifted in/out serially at a rate equal to the clock frequency of 2MHz. The LDVD output is transmitted on the rising edge and the receiver samples the LUVD input on the falling edge of the clock. The CENN controls have effect only after the current bit in the packet is transmitted/received.

(1) Microprocessor Read Cycle

Read Timing internal register of IC303 by Microprocessor is shown in Timing 4 - 15.

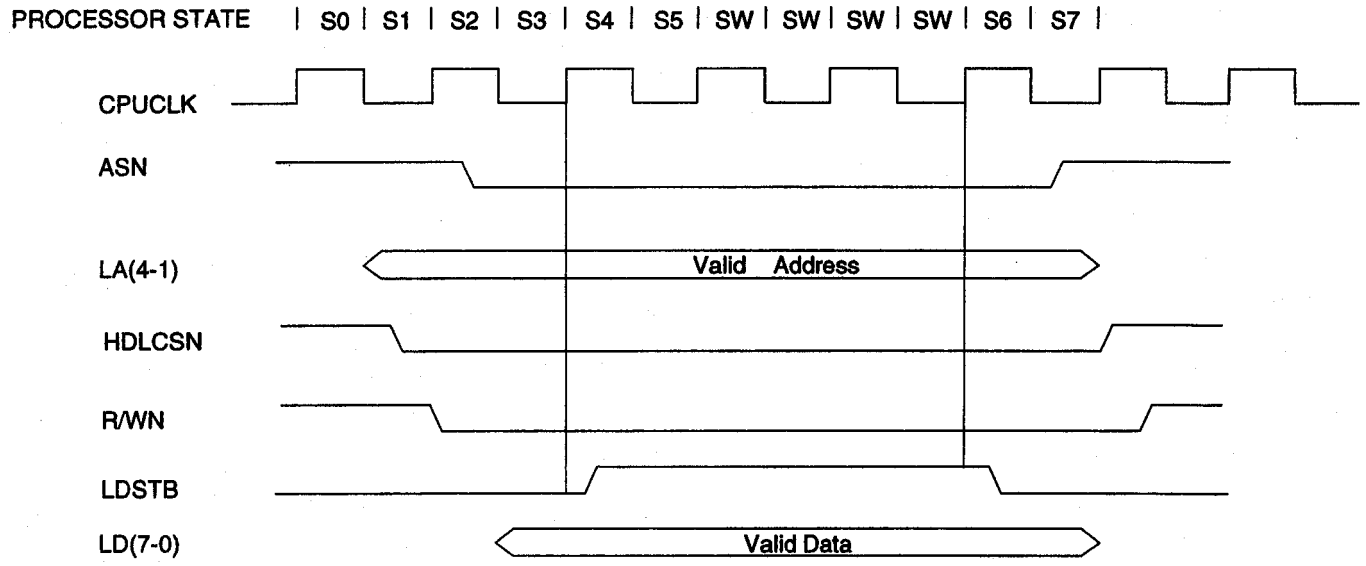


Timing 4-15. D-PITS Protocol Controller Read Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to LA(4 - 1) in S1 state while holding R/WN High. System Controller (IC302) asserts HDLCSN in Low. System Controller asserts LDSTB High in S2 state. LDSTB is asserted in High, R/WN is in High = read condition, IC303 outputs the condition of internal register corresponds with LA (4 - 1) at that time to LD (7 - 0). Microprocessor takes in effective data on LD(7 - 0) in the falling edge of S6 state.

(2) Microprocessor Write Cycle

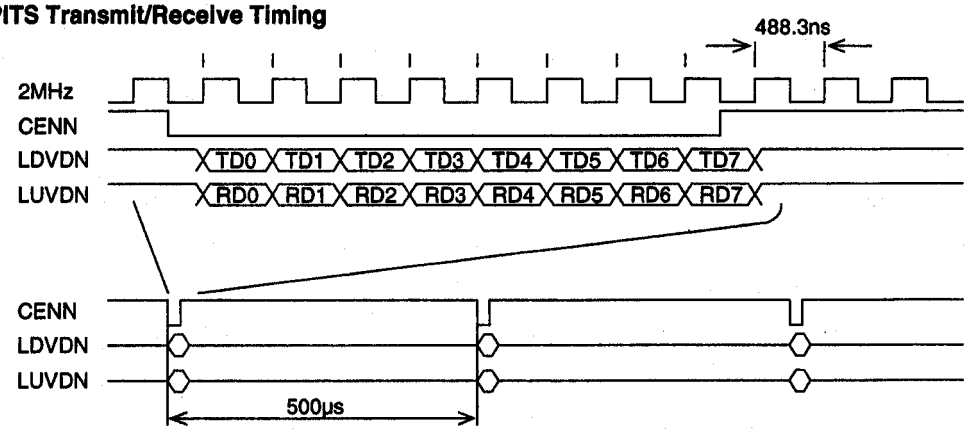
Write Timing internal register of IC303 by Microprocessor is shown in Timing 4 - 16.



Timing 4-16. D-PITS Protocol Controller Write Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to LA(4 - 1) in S1 state. System Controller (IC302) asserts HDLCSN in Low. Microprocessor asserts R/WN in Low = Write in S2 state, then from S3 state it outputs an effective data to LD (7 - 0). System Controller asserts from the period of the rising edge in S4 state to the rising edge of S6 state LDSTB High. IC303 takes in the condition of LA (4 - 1) in the rising edge of LDSTB and writes on the internal register effective data corresponds with LA (4 - 1) internal register in the falling edge of LDSTB .

(3) D-PITS Transmit/Receive Timing



Timing 4-17. D-PITS Transmit/Receive

D-PITS Transmit/Receive Timing is shown in Timing 4 - 17.

D-PITS transmit data (LDVDN) shifted out from IC303 in the rising edge of 2MHz is sent out though IC319 to the DSP card. D-PITS reception data (LUVDN) input from the DSP card is input though IC319 to IC303, then sampled in the falling edge of 2MHz. While an effective D-PITS data exists on the signal line of LDVDN and LUVDN, CENN is asserted in low by the System Controller (IC302).

CENN is asserted by system Controller in the falling edge of 2MHz, and negated in the falling edge after 8 clock cycles. IC303 shifts out effective transmit data to LDVDN in the rising edge of 2MHz. Effective transmit data is from the rising edge of 2MHz right after CENN is asserted to the rising edge right after CENN is negated. Moreover, IC303 samples an effective reception data from the falling edge of 2MHz right after CENN is asserted to the falling edge right after CENN is negated on LUVDN in the falling edge of 2MHz. Data Packet is input and output every 8 bits to the Protocol Controller. The cycle is 500µs.

1-9. Hard Disk Interface

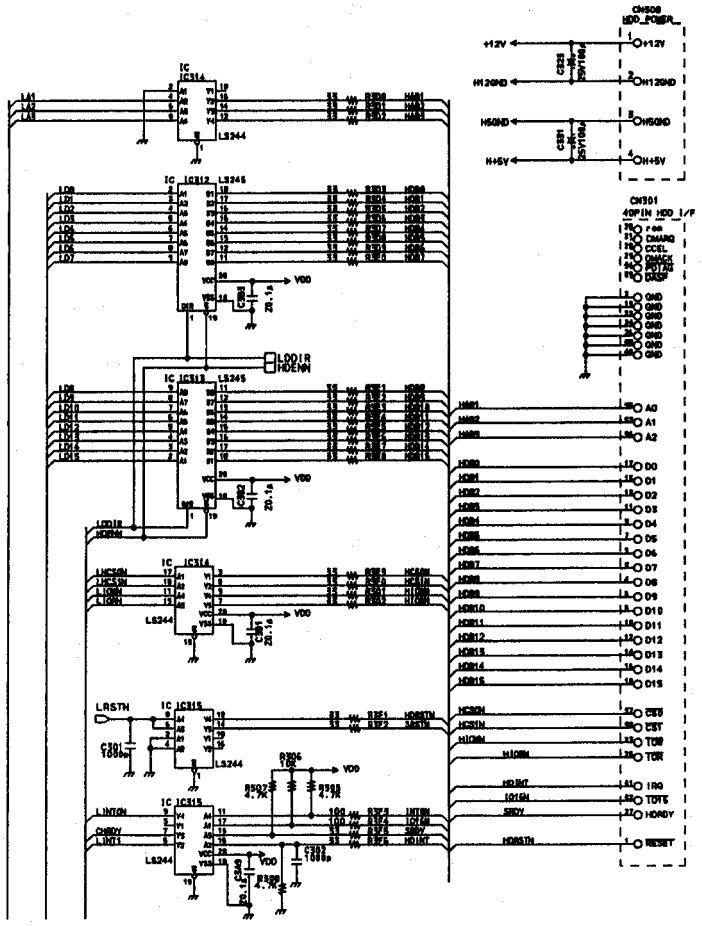


Fig. 4-13. Hard Disk Interface

The Hard Disk Drive used in the VPS installs an intelligent interface built-in disk controller. CPU Card's Interface circuit is shown in Figure 4 - 13. The Hard Disk interface allows parallel data to transfer between the Hard Disk Drive and a Microprocessor bus. This interface consists of a Data Bus (D15 - D0), Address Bus (A2 - A0), Chip Select (CS0, CS1) and 6 control signals (IOR, IOW, IRQ, IO16, HDRDY, RESET). The VPS does not use HDRDY and IO16 signals. The Hard Disk Interface Connector's pin Assignment is shown in Table 4 - 1.

Table 4-1. Hard Disk interface Pin Assignment

Pin No.	Signal Name	Pin No.	Signal Name
01	-HOST RESET	02	GND
03	+HOST DATA 7	04	+HOST DATA 8
05	+HOST DATA 6	06	+HOST DATA 9
07	+HOST DATA 5	08	+HOST DATA 10
09	+HOST DATA 4	10	+HOST DATA 11
11	+HOST DATA 3	12	+HOST DATA 12
13	+HOST DATA 2	14	+HOST DATA 13
15	+HOST DATA 1	16	+HOST DATA 14
17	+HOST DATA 0	18	+HOST DATA 15
19	GND	20	KEY
21	+DMARQ	22	GND
23	-HOST IOW	24	GND
25	-HOST IOR	26	GND
27	+IOCHRDY	28	+CSEL
29	-DMACK	30	GND
31	+HOST IRQ14	32	+HOST IO16
33	+ADDR1	34	+HOST PDIAG
35	+ADDR0	36	+ADDR2
37	-HOST CR0	38	-HOST CR1
39	-DAST	40	GND

(1) Hard Disk Interface Signals Descriptions

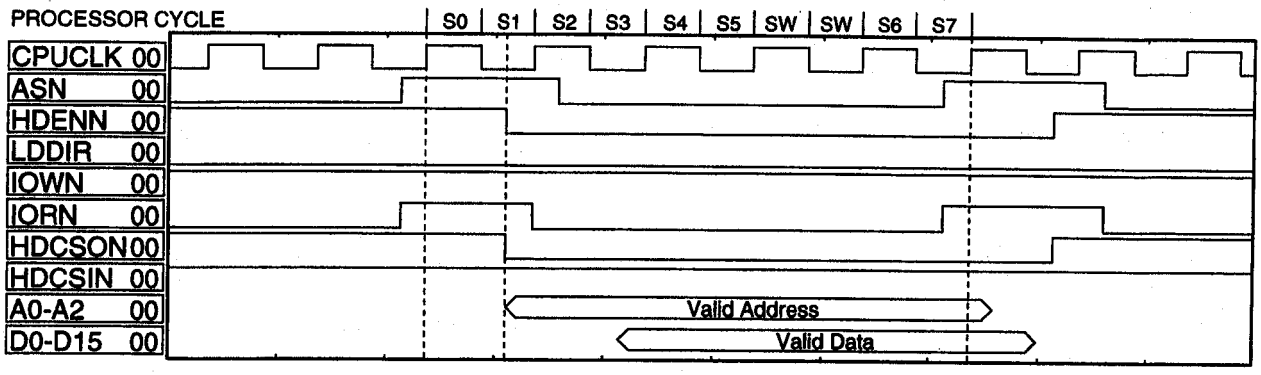
Signal Name	Pin No.	Input/Output	Explanation
-RESET	1	O	Reset signal from host system. Power source of host system turns on, becomes active.
GND	2, 19 22, 24 26, 30 40, 43	O	Ground
DATA 0 - 15	3 - 18	I/O	16 bit mutual direction data bus. Low-ranking 8 bit (DATA 0 - 7) is transferred when it gains access to registers except for the data register and ECC data inside the data register.
KEY Pin	20		Key pin to prevent cable connector from incorrect insertion. on drive side is broken off and removed, then inserted in the pin on the cable side.

Signal Name	Pin No.	Input/Output	Explanation
-10W	23	O	Write strobe signal. When drive select signal (-CS0.1) is active, data on data bus is written in the register inside drive by the Trailing Edge.
-10R	25	O	Read strobe signal. When drive select signal (-CS0.1) is active, data inside the register is output onto the data bus with low active, then it is read into the host system with Trailing Edge.
IRQ	31	I	Interrupt signal to host system. It is active when drive is selected, and -IEN (Interrupt Enable) inside flexed disk register is active. Generated interrupt phenomenon or not it becomes high- impedance status except when the above condition occurs. IRQ signal is reset when host system reads status register or command is written in the command register.
RESERVED	21, 27 28, 29 44		Reserve Signal. Non-connecting condition.
-IO16	32	I	The signal (Open drain) informs the 16 bit data transferred mode (16 bit data register is gained access). (Not used)
-PDIAG	34	I/O	Used to inform master drive of the existence of slave drive and to receive and send the result of the diagnostic com mand between the master and slave drive. (Not used)
A0, A1, A2	35, 33, 36	O	Address decode signal of internal register.
-CS0	37	O	Chip select signal. To select one group within two internal register groups.
-CS1	38	O	Chip select signal. To select one group within two internal register groups.
-DASP	39	I	During drive access (from receiving command to command end), it becomes active. Used to drive external LED. Composing Master/slave, it is used to inform master drive of the existence of the slave drive. (Not used)
+5V (LOGIC)	41	O	Power source of logic group • analog group
+5V (MOTOR)	42	O	Power source of motor driving.

* The signal from drive to host system is I (Input), from host system to drive is O (output).

(2) Microprocessor Read Cycle

Read Timing from the internal register of the Hard Disk by Microprocessor is shown in Timing 4 - 18.

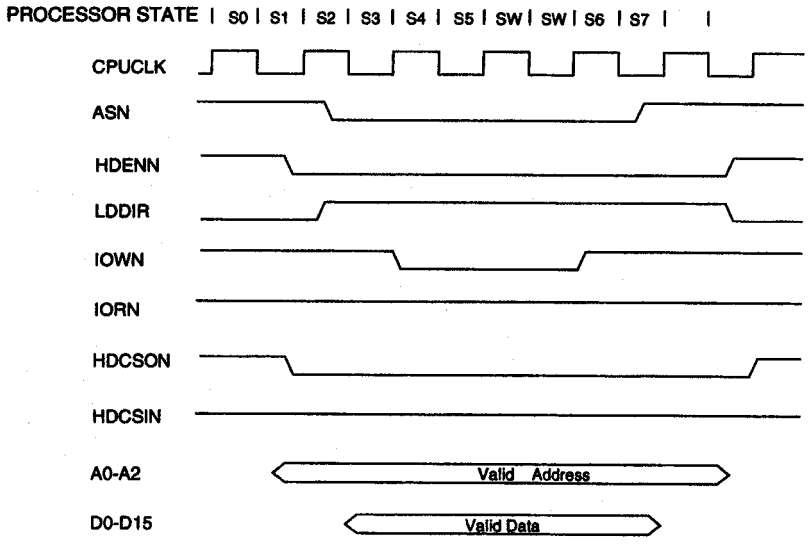


Timing 4-18. Hard Disk Read Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to A(2 - 0) in S1 State. System Controller (IC302) asserts either HDCSON or HDCSIN. System Controller asserts IORN low in S2 state. Hard Disk outputs the condition of internal register correspondence with A(2 - 0) IORN in time IORN is asserted to D(0 - 15). The Microprocessor takes effective data on D(15 - 0) in the falling edge of S6 State. In Read Cycle, IC312/IC313 (L5245 Bus Tranceive) is the Control Signal. HDENN (IC312/IC313, pin 19) is asserted in low in the period from S1 state to S7 state. LDDIR (IC312/IC313, pin 1) is asserted in low.

(3) Microprocessor Write Cycle

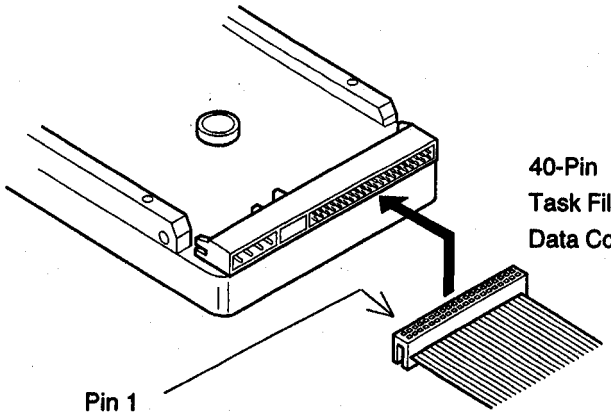
Write Timing to the internal register of the Hard Disk by Microprocessor is shown in Timing 4 - 19.



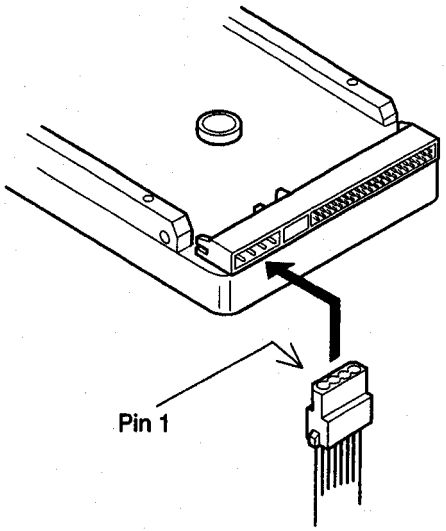
Timing 4-19. Hard Disk Write Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to A(2 - 0) in S1 State. System Controller (IC302) asserts either HDCSON or HDCSIN. Microprocessor outputs effective written data onto D(15 - 0) in the period from S3 state to S7 state. System Controller is asserted in low in the period from the rising edge of S4 state to rising edge of S6 state. Hard Disk takes effective data on D(15 - 0) inside by the rising edge of IOWN. In Write Cycle HDENN(IC312/IC313 - pin 19) , Control Signal of IC312/IC313 (LS245 Bus Transceiver), is asserted in low in the period from S1 state to S7 state. LDDIR (IC312/IC313 - pin 1) is asserted in low in the period from S2 state to S7 state.

4) Attaching a Data Cable to the Drive



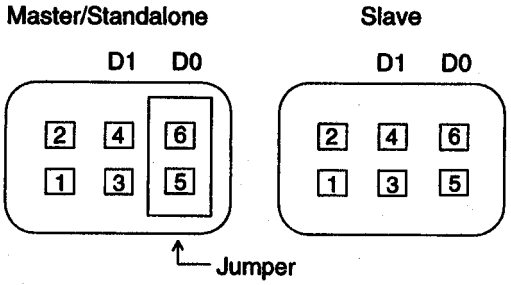
5) Attaching a Power to the Drive



Pin	signal
1	+12 Volts
2	GND
3	GND
4	+5Volts

The jumper settings differ according to the hard disk drive used. For details, refer to the specifications manual of the hard disk drive.

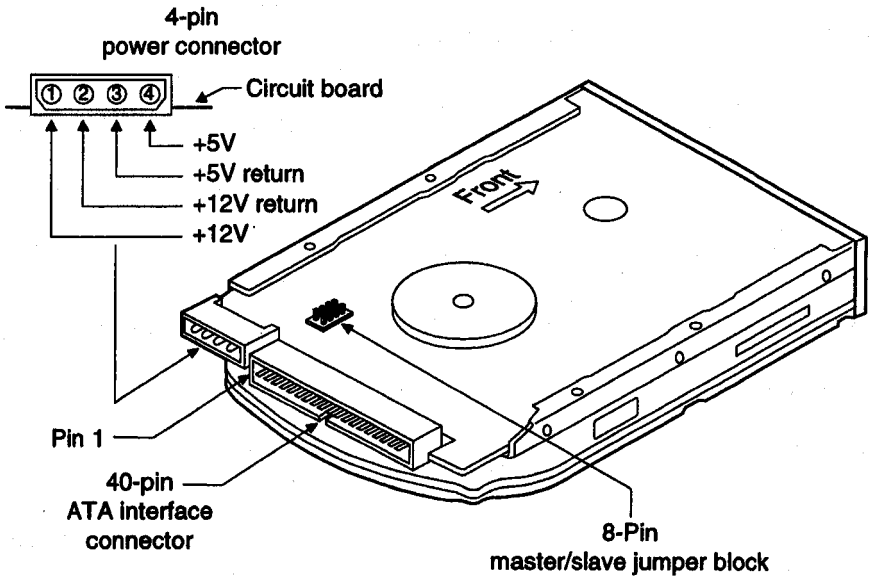
6) Setting the Drive's Jumpers (Manufactured by SEAGATE, ST31276A)

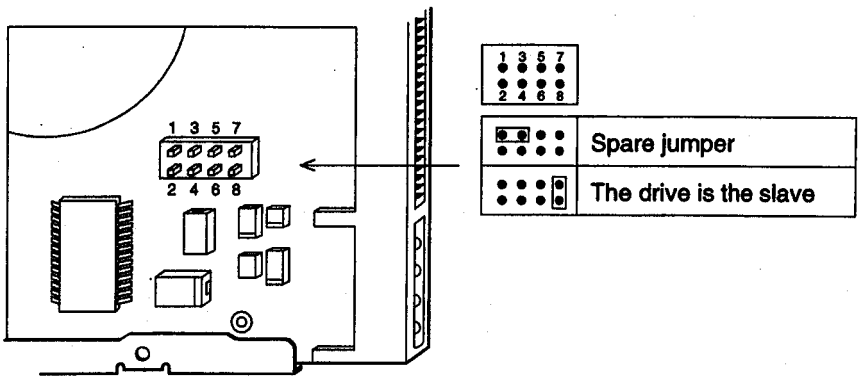


Here is how you can set these jumpers. Pins described as "resered" should not be used.

D1(Pins 3&4)	D0(Pins 5&6)	Desciption
Open	Open	Slave
Open	Closed	Master
Closed	Open	Cable Select enabled
Closed	Closed	Master W/forced Slave present

7)Setting the Drive's Jumper (Manufactured by SEAGATE, ST3850A)





1-10. Extension Bus (DSP Card Interface)

The Expansion Bus has two ports. The serial port transmits and receives the voice data and the parallel port provides a Microprocessor interface for access to various registers in the add-in card. The CPU Card distributes the Bus signals to 3 expansion connectors (CN302, CN303, CN304).

(1) Add in Card Selection Signals

The CPU Card provides these connectors Slot ID Signal composed by S(2 - 0). SL(2-0) is used in case of gaining access to add-in Card mounted by Expansion Connector, to select a card from others. The Add-in Card mounted to Expansion Connector compares the value of SL(2 - 0) provided from the connector with a part of destination address = ESA(2 - 0) provided by Microprocessor. The result of the comparison is considered by the add-in card condition of card selected. In this VPS, "000" for CN302 = slot 1, "010" for CN303 = slot 2 and "100" of slot IC = SL(2 - 0) for CN304 = slot 3 are provided.

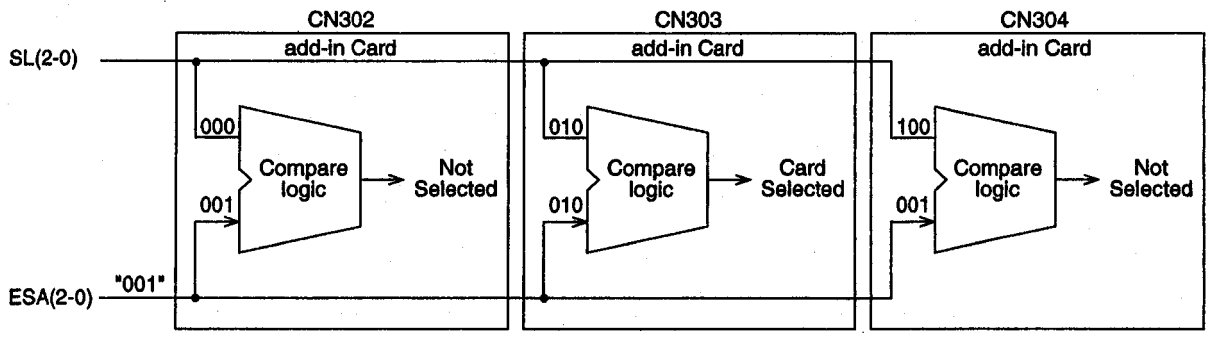


Fig. 4-14. Card Selection Logic for the Expansion Bus

(2) Microprocessor Port

The Microprocessor Port allows 8 bit parallel data transfers between the various registers on the add-in card and a Microprocessor on the CPU Card. This interface consists of a Data Bus(DB7 - DB0), Address Bus (AB6~AB1) Card Select (SL(2 - 0), ESA (2 - 0), IOSN), 2 Control Signals (LDSN, RWN) and 3 miscellaneous signals (SRSTN, IORDY, INTON, SCLK). Table 4 - 2 describes the Microprocessor Port.

Table 4 - 2. Microprocessor Port of the Expansion Bus

Signal Name	Pin No.	Input/Output	Explanation
DB (7 - 0)	10 ~ 3	I/O	8 bit bidirectional Data Bus. This data bus allows data transfer between I/O port in the add-in Card and a Microprocessor.
AB (06 - 01)	18 ~ 13	O	6 bit output Address Bus. These bits address the various registers in the add-in card. They select the internal registers in conjunction with card select and control signals.
ESA (2 - 0)	23 ~ 21	O	3 bit expansion Slot Address Bus. These bits address one expansion Slot within other expansion slots.
SL (2 - 0)	36 ~ 34	O	3 bit expansion slot identity output. These bits are given to each expansion slot. It shows a unique slot number.
IOSN	24	O	Card Select output. This is an active low output, enabling the read or write operation to various registers in the add-in card.
LDSN	27	O	Lower byte Strobe output. This output activates the Address Bus and RWN output and enables data transfers on the Data Bus.
RWN	28	O	Read Write Control output. This output controls the direction of data flow on the data bus. When High, the I/O buffer acts as an output drive and as an input buffer when low.
SRSTN	33	O	System Reset Output. This is an active low output, resetting all the registers in the add-in card.
INTON	30	I	Interrupt Request input.(Open Collector) This active low input notifies the controlling Microprocessor of an interrupt request.
IORDY	29	I	IO Data Ready input (3 state) This active High input indicates the current bus cycle is complete. If the add-in card negates this signal at the current bus cycle, when the Microprocessor addresses the slower device on the add-in card, the current bus cycle waits until IORDY asserts to High.
SCLK	37	O	System Clock output. This clock output is the same as SPUCLK (12.288MHz).

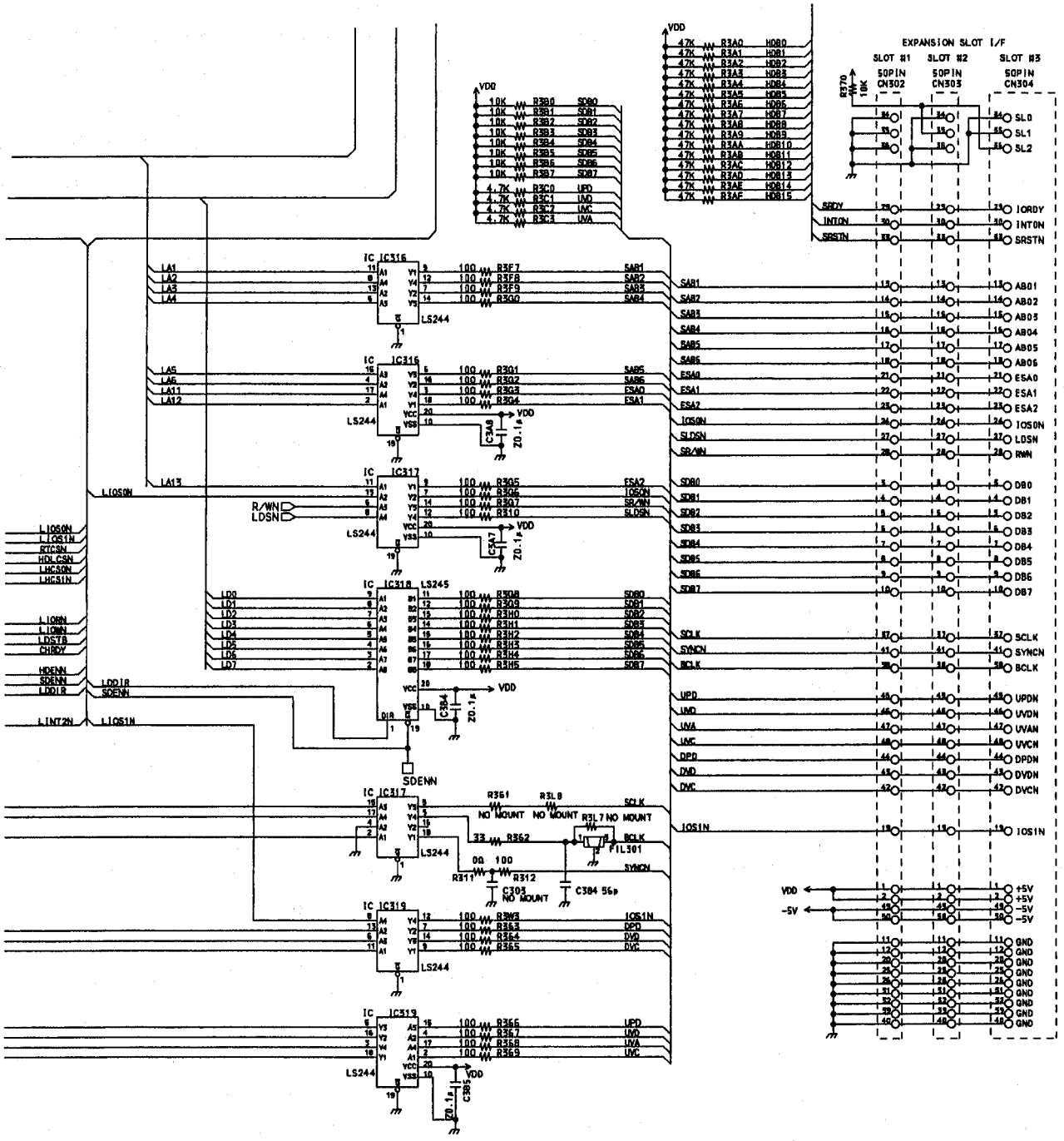
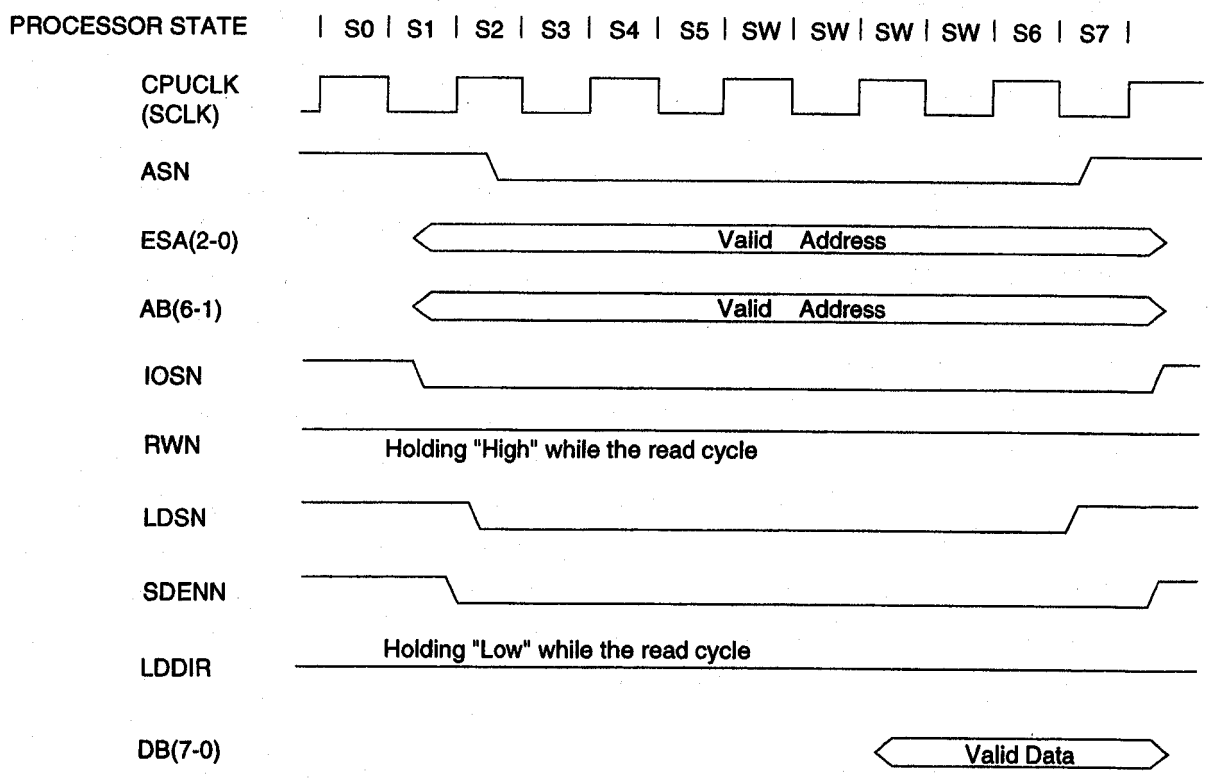


Fig. 4-15. Expansion Bus Interface

(3) DSP Card Read Cycle By Microprocessor

Read Timing of the DSP Card by Microprocessor is shown in Timing 4 - 20.



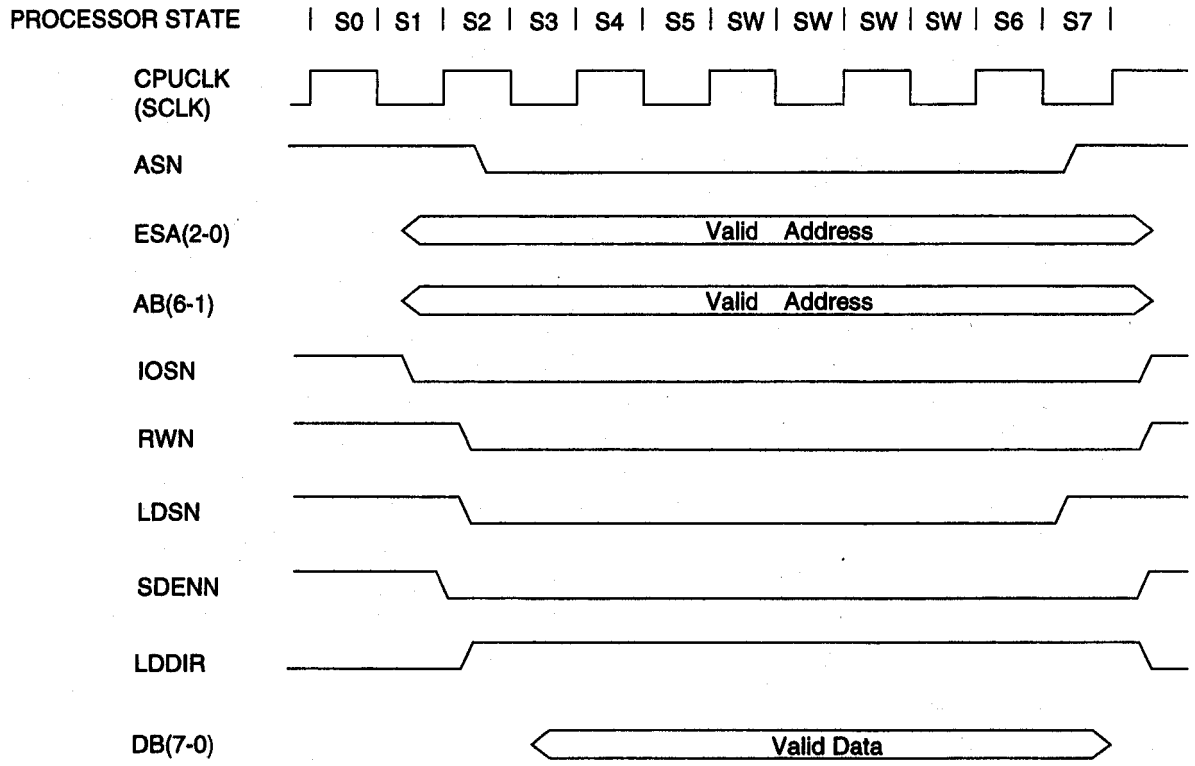
Timing 4-20. DSP Card Read Cycle by Microprocessor

The Microprocessor (IC301) outputs Valid Address to ESA (2 - 0) in S1 State. System Controller (IC302) asserts IOSN in low. Microprocessor holds RWN High, asserts LDSN in low, in the period from the rising edge of S2 state to the falling edge of S6 state. DSP card outputs the register condition corresponding with AB (6 - 1) and ESA (2 - 0) to DB (7 - 0). Microprocessor takes effective data on DB (7 - 0) in the falling edge of S6 state. In Read Cycle SDENN (pin 19), control signal of IC318 (LS245 - Bus Tranceiver) is asserted by system controller in the period from S1 State to S7 State in low. LDDIR (1 pin) is asserted in low.

(4) DPS Card Read Write By Microprocessor

Write Timing of DSP Card by Microprocessor is shown in Timing 4 - 21.

Microprocessor (IC301) outputs Valid Address to AB (6 - 1) and ESA (2 - 0) in S1 State. System Controller (IC302) asserts IOSN in low. Microprocessor asserts RWN in S2 State in low, and outputs write data from S3 state onto DB (7 - 0). Microprocessor asserts LDSN in lo w in the period from the rising edge of S2 state to the falling edge of S6 State. DSP card takes effective data on DB (7 - 0) in the rising edge of LDSN. In Write Cycle SDENN (pin 19), control signal of IC308 (LS245 - Bus Tranceiver) is asserted by the system controller in the period from S1 State to S7 State in low.



Timing 4-21. DSP Card Write Cycle by Microprocessor

(5) Overview of the Serial Voice Port

Voice Port lessens the connecting signal line between the CPU and DSP Card. This time-share serial bus is designed to realize transmitting sufficient data in its performance. The Control section on the host (CPU) side is the master controller and the control section on the DSP card side is the slave controller.

Data for two kind of 32 channels passes through on this bus. Data types are ADPCM VOICE Data (32kBPS/CH) and D-PITS Data (max 32kBPS/CH). The Time slot passes through individual data called VOICE Channel and PITS Channel.

•Voice Channel

Voice Channel is a serial bus with bit rate : 2MHz and practice data transfer ability : 32 kBPS, and each individual channel is in the 32 time- share. Normally ADPCM compressed voice data is passing through.

DMA data transfer method is offered by Voice Channel. The cooperation DMA channel inside the slave controller and bus masterlogic inside the master controller makes it possible for DMA data between the voice buffer inside the controller and host memory to transfer.

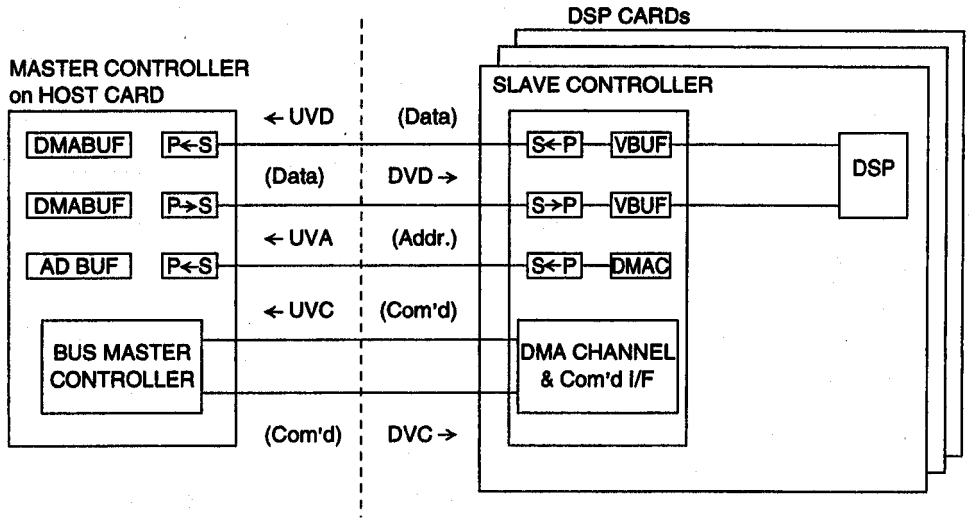


Fig. 4-16. Voice Channel on the Voice Port

In DSP/COL Card Module, voice Band digital data is received from the circuit : T-R line is input by DSP, and DSP executes voice data's ADPCM compressing disposition. Compressed ADPCM data is stored in the voice buffer inside the slave controller by DSP. Voice Channel transfers DMA to host memory by the speed of 32kBPS/channel.

In time recording disposition (voice compression) ADPCM data stored by DSP in the voice buffer inside the slave controller, data transfer and address information, and DMA channel inside the slave controller, are output to the voice channel. Based on this information, master controller drives inside its bus master logic, holding CPU, then stores ADPCM data input from Voice Channel on host memory.

In play-back disposition, ADPCM data on host memory is stored in the voice buffer inside the slave controller from the voice channel. ADPCM data inside the voice buffer is restored to voice band digital data by DSP, and sent out to the line : T-R line.

In this playback disposition, data transfer information and address information generated by the DMA channel inside the slave controller are output to the voice channel. Based on this information, master controller drives in its bus master logic, holding CPU, then transfers ADPCM Data from host memory to the Voice channel buffer inside master controller. The data stored in the Voice channel buffer is transferred to the VOICE channel buffer inside the master controller through the voice channel. DSP takes over ADPCM from this voice buffer.

•PITS channel

PITS Channel is a time-share bus of 2MBPS and 16 bitx32channels. It realizes transmitting data between D-PITS buffer inside the slave controller and HDLC controller on the CPU card. The data, sent and received in D-PITS buffer inside the slave controller through the PITS channel, is sent and received by the PBX through interface logic.

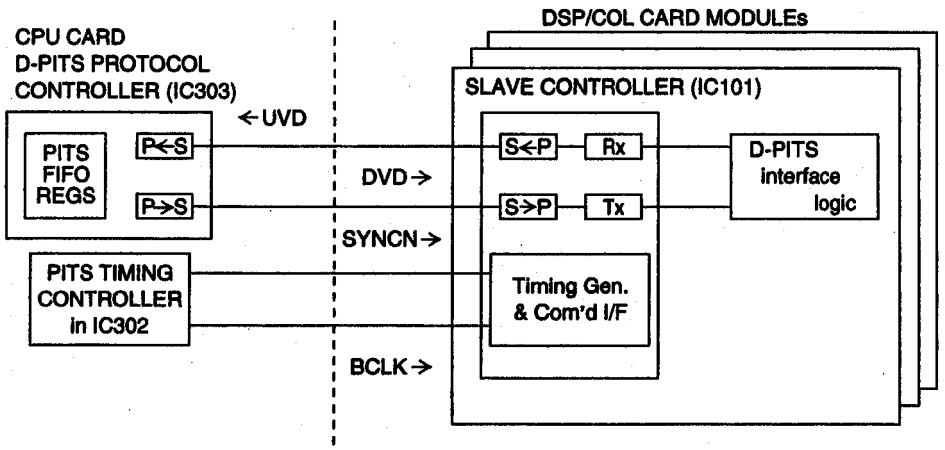


Fig. 4-17. PITS Channel on the Voice Port

When receiving and sending D-PITS data, data transfer between the D-PITS protocol controller (IC303) on the host card and the PITS buffer inside the slave controller (IC101) is realized. PITS control logic inside the master controller (IC302) controls the receiving and transfer timing of the D-PITS protocol controller on the host card. The data channel component is extracted from the D-PITS data received from the circuit line by interface logic, then stored in the PITS-RX buffer inside the slave controller. D-PITS data stored in the PITS-RX buffer inside the slave controller is input in the D-PITS protocol controller on the host card through the PITS channel. The PITS-RX buffer size inside the slave controller is 8 bit.

D-PITS data to be sent out from the circuit line is stored in the PITS-TX buffer inside the slave controller from the D-PITS protocol controller through the PITS channel. D-PITS data stored in the PITS-TX buffer is symbolized by interface logic and output from the circuit line. The PITS-TX buffer size inside the slave controller is 8 bit.

(6) The Frame Format of the Voice Port

Voice Port is composed by five lines, SYNCN (Synchronization pulse) directs master controller ' slave controller (down road), BCLK (Bit Clock), DVD (Download-Voice-Data), DVA (Download-Voice Address) and DVC (Down load-Voice command), two signal lines, and UVD(Upload-Voice-Data) directs master controller (up load) and UVC (Upload-Voice-Command).

Master controller outputs frame pulse (SYNCN : 2kHz) and Base Clock (BCLK : 4.096MHz) to the slave controller for synchronization.

Voice Port is 500us/32 channel time share bus, synchronized with SYNCN generated from the Master Controller. One frame of the voice port is 500us and VOICE/PITS DATA of 32 channels pass through time share. VOICE/PITS DATA maximum 1x32 channel/frame can pass through one frame period. Each VOICE Channel/ PITS channel is composed of 488ns/bit (2.048MHz) x 16bit (=7812ns), the arrangement of each channel is from the head VOICE channel:0, PITS channel:0, VOICE channel:1, PITS channel1, ..., VOICE channel:31, PITS channel :32.

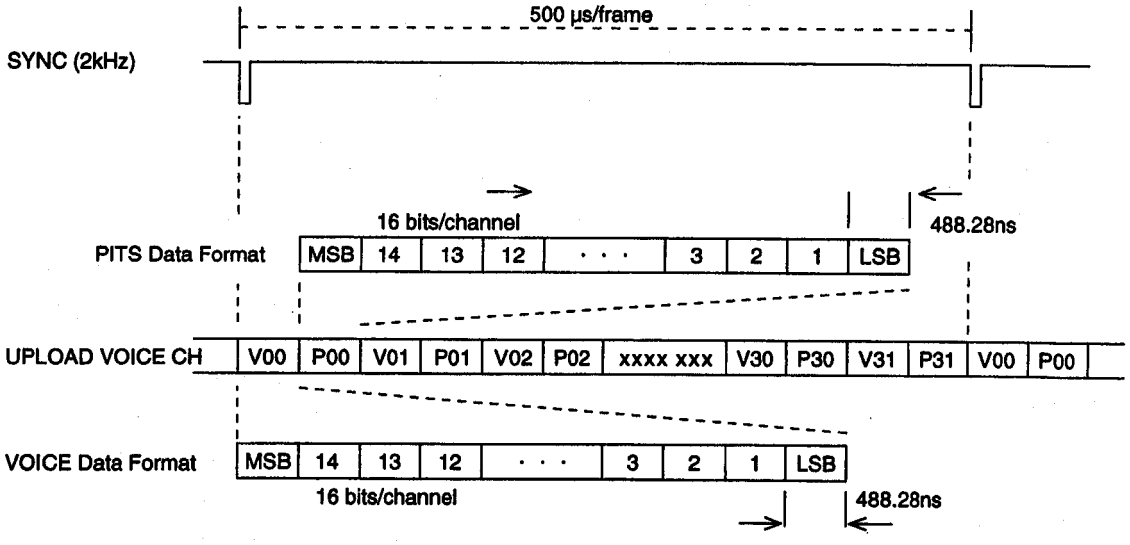


Fig. 4-18. Voice Port Timeslot Assignment

Host CPU programs the slave controller. The slave controller assigns the channel which can be used. Time slot logic inside the slave controller, corresponds with this channel assignment, decides the channel slot available for itself and make required control signals from the frame pulse and 4MHz clock.

In VOICE channel, down load timing is behind the time for 64 bit (31.24usec) in regard to up load timing. Voice channel offers a DMA transmitting method. For this reason, command reception of the master command and latency for direct memory access are added.

In case of down loading play back data from the host memory to the DSP card using DMA data transfer; eg, VOICE data, responded to DMA data transfer command up-loaded in CH0, is down loaded in the timing of CH2. VOICE channel defines each channel, up-loaded at the time SYNC is being asserted, as CH0, thereafter, CH1, CH2,...CH31.

PITS channel has no DMA data transfer function. Referring to external-fixed HDLC controller and interface, up load channel and down load channel are the same timing.

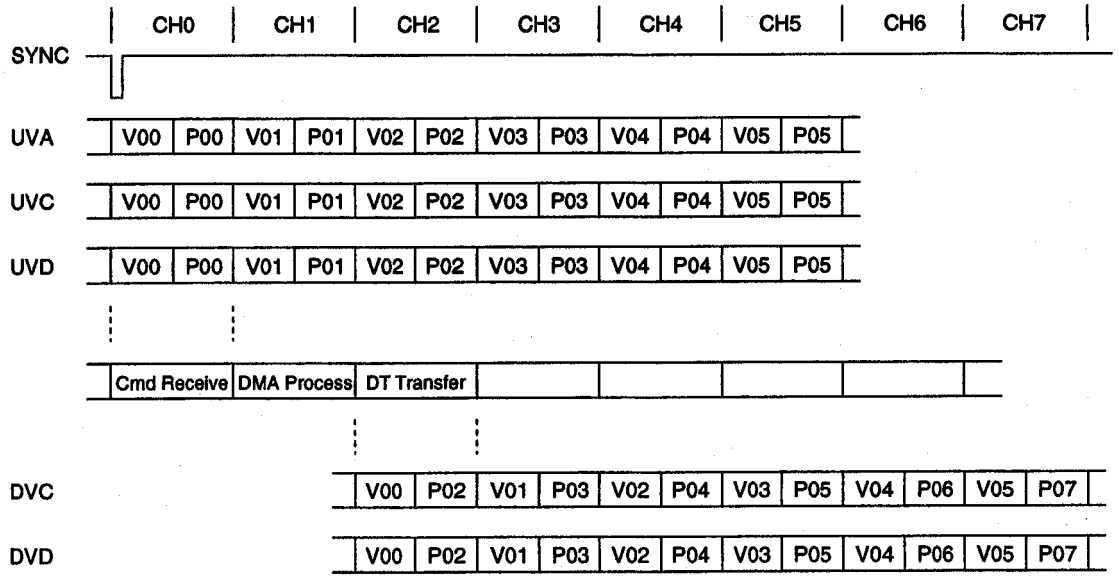


Fig. 4-19. Voice Port Frame Format

(7) The Data Format of the Voice Port

•VOICE CHANNEL Data Format

Format of the VOICE channel in up load channel is defined as follows.

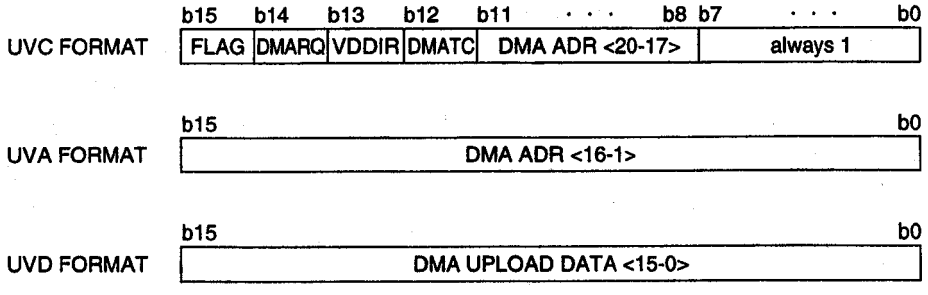


Fig. 4-20. Voice Channel Upload Data Format

FLAG bit of command channel is a signal that indicates the DMA channel inside the slave controller to start transmitting effective data and Low assert.
DMARQ bit is a DMA request signal, against the DMA channel inside the slave controller. It asserts when DSP on the DSP card requests host memory to transfer DMA data and it is in Low assert. The Master controller motivates the DMA data transfer process for the channel and its main bit is asserted.
DMATC bit is a TC (Transfer Complete) signal asserted when the number of times the DMA channel inside the slave controller executed, reaches the regulated number of times and low assert. This bit is asserted only once when it reaches TC, this bit is latched the inside master controller and informed to the host CPU as a DMATC intrusion.
DMA ADR(20 - 1) bit, divided in the command and address channel, is an address on system memory existing as ADPCM data.
DMA DATA (15 - 0) allotted to the data channel is up load data to be a DMA object. This data is ADPCM voice data to be stored in system memory, compressed on the DSP card.

The mode of DMA can be divided into two groups because of the direction of the DMA transfer.

First, in the case of the DSP card ' host memory; data is transferred from a 16 bit voice buffer inside the slave controller to a DMA data buffer inside the master controller. The Slave controller is asserted as DMARQ to command channel, DMA address is placed on the address channel, and data is placed on the data channel. Then these are transferred to the master controller. Master controller stores transferred command/ address/data in a DMA buffer temporary, then requires the host CPU to hand over Bus Ownership. When host CPU releases, the bus master controller executes a transfer from DMA buffer to host memory.

Second, in the case of host memory ' I/O card, data is transferred from a 16 bit DMA data buffer inside the slave controller to a voice buffer inside the I/O card. Slave controller is asserted as DMARQ to the command channel, DMA address is placed on the address channel, then these are transferred to master controller. Master controller stores transferred command/address/data in a DMA buffer temporarily, then requires the host CPU to hand over Bus Owner ship. When host CPU releases, the bus master controller reads data from the host memory, in the next phase through up load bus transfers data to slave control.

Mode phase of the VOICE channel by up load command is as follows.

TYPE OF UPLOAD COMMAND				
DWAIT	DMARQ	VDDIR	DMATC	FUNCTION
0	0	0	1	HOST → I/O CARD DMA Request
0	0	1	1	I/O CARD → HOST DMA Request
0	0	0	0	HOST → I/O CARD DMA Request with TC flag
0	0	1	0	I/O CARD → HOST DMA Request with TC flag
1	x	x	x	idle State

Format of down load channel is defined as follows.

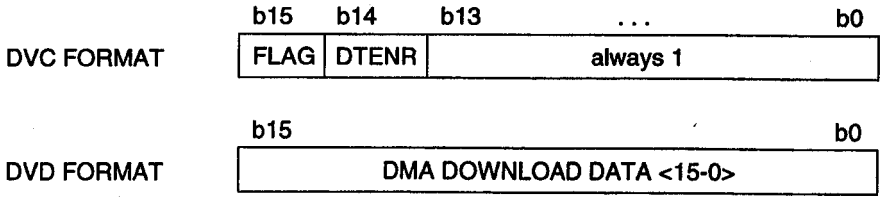


Fig. 4-21. Voice Channel Download Data Format

The Down load channel has only a command channel and data channel.
FLAG bit of the command channel is a signal indicating the master controller to start effective data transfer, and low assert.
The meaning of DTENB bit differs with the direction of data transfer.
In master controller'slave controller direction transfer; it is indicated that data on the data channel sent by the master controller is the same as the data on the host memory requested from the DSP card.
Slave controller'master controller direction controller, it is indicated that effective data sent from the slave controller is stored in system memory. This bit is low assert.

DMA transfer direction is host ' DSP card; the effective data should be transferred from a 16 bit DMA data buffer inside the master controller to a voice buffer inside the slave controller. Master controller stores DMA address sent from the DMA channel inside the slave controller together with a DMA request in the DMA buffer temporarily, then requires host CPU to release bus. When host CPU releases, master controller reads data from host memory, then transfers effective data to the slave controller through the down load channel in the following phase.

Motion phase of VOICE channel by down load command is as follows.

TYPE OF DOWNLOAD COMMAND		
START	DMAEN	FUNCTION
0	0	Requested DMA Transfer Succeed
1	x	idle State

•PITS CHANNEL data Format

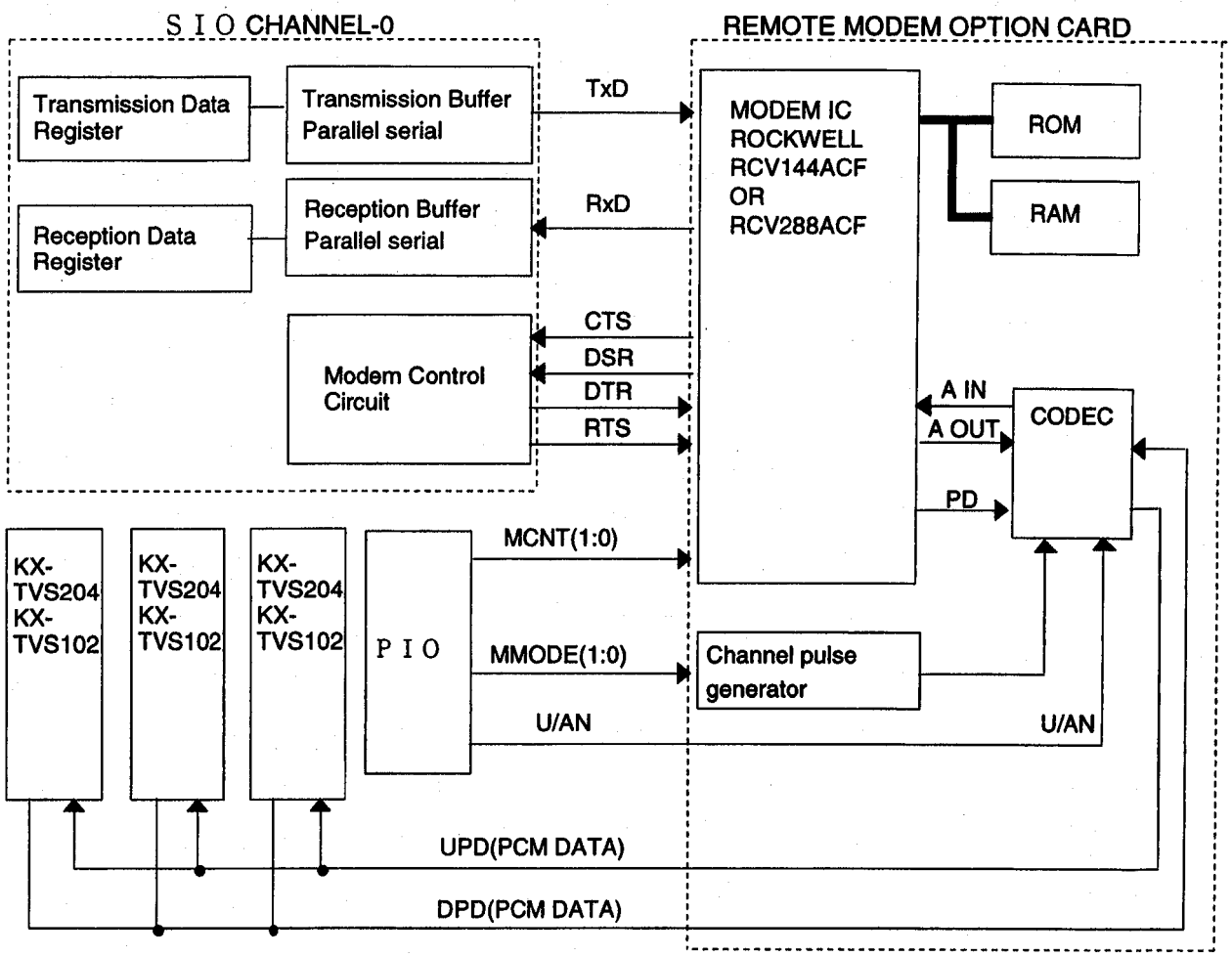
PITS channel uses only data line and its format is defined as follows.

	b15 ... b8	b7 ... b0
DVD FORMAT	D-PITS DOWNLOAD DATA <7-0>	not defined
UVD FORMAT	D-PITS UPLOAD DATA <7-0>	not defined

DATA (7 - 0) allotted to the down load channel indicates D-PITS DATA to be sent to the PBX, DATA (7 - 0) allotted to the up load channel indicates D-PITS data received from the PBX.

1-11. Remote Modem Interface(Future Option)

The KX-TVS200 has a remote modem interface which uses serial I/O channel #0 of the CPU.
General diagram of remote modem interface.



The remote modem option card is configured as shown in the figure above. It is controlled by part of the serial interface and parallel interface of the host CPU.
The voice data of the PCM voice data highway, which is supplied to the CPU circuit board from the KX-TVS102 or KX-TVS204 line module, is converted into analog signals by the codec on the modem card and input to the modem IC. The modem IC converts the modem signals into data using the modem communication protocol supplied from Rockwell. The host CPU uses the serial I/O port to transfer data to and from the modem IC.
Using the parallel I/O port (2 bits) of the host CPU, the connection of the line channels with the modem can be switched. However, this switching is done on a slot by slot basis, and connection is made with the lowest channel number of the line modules installed in the expansion I/O slots. For instance, when the KX-TVS204 modules have been installed in three slots, CH1 (slot 1), CH5 (slot 2) or CH9 (slot 3) among the 12 channels is selected as the channel which can be connected to the modem.
μ law or A law can be selected for the codec using the parallel I/O port (1 bit) of the host CPU. The host CPU must select μ law or A law in synchronization with the selection of the country code.
The modem test mode can be selected using the parallel I/O port (2 bits) of the host CPU. The test modes include the analog loop test mode and remote digital loop select mode. Reference should be made to the Rockwell RCV288ACF/RCV144ACF Specifications Manual for further details.
The power-down control of the codec is linked with the off-hook signal (0H) which is output from the modem IC. The host CPU must input the appropriate command using the serial I/O port so as to exercise control in such a way that the power to the codec is turned on when the modem is used.
The parallel I/O port for controlling the modem is now described.
The port for connection with the modem is set using parallel I/O bits 2 and 3.

Signal Name				
PIO bit(2):MMODE0	1	0	1	0
PIO bit(3):MMODE1	1	1	0	0
connection channel	CH#1	CH#5	CH#9	not use

The modem test mode is set using parallel I/O bits 9 and 10.
The μ law or A law is selected using parallel I/O bit 8.

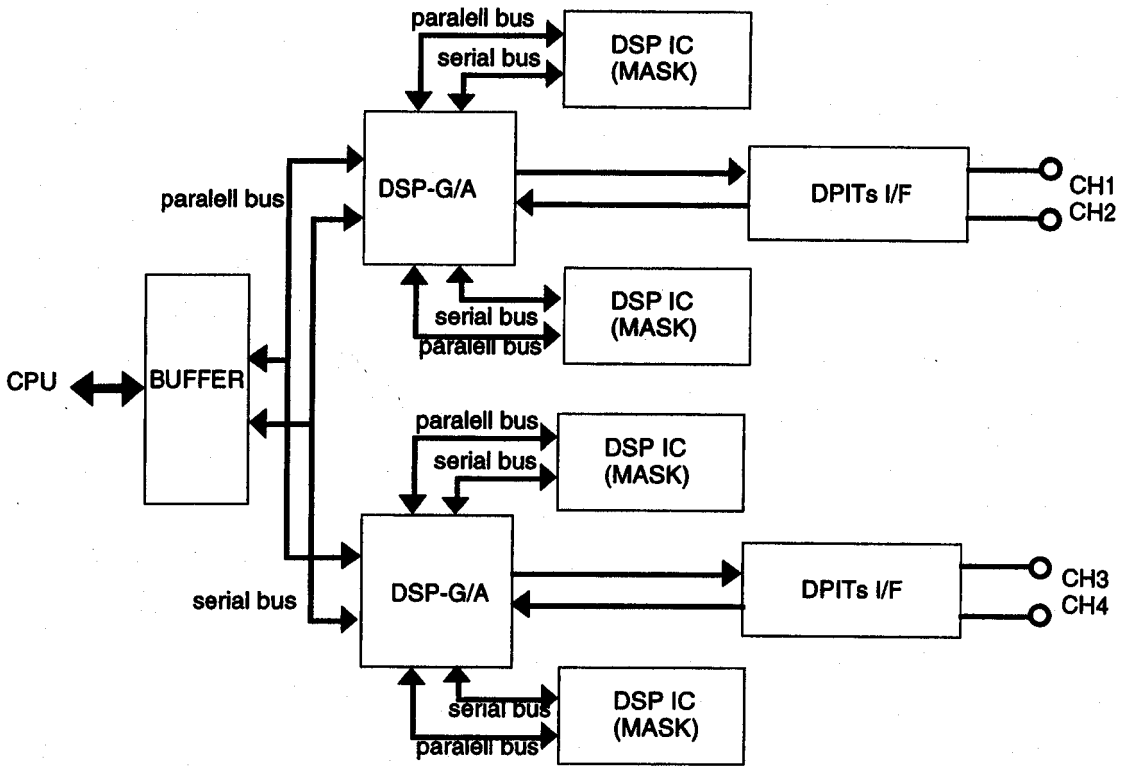
Signal Name				
PIO bit(9):MMODE0	0	1	0	1
PIO bit(10):MMODE1	0	0	1	1
Test Item	not use	Remote digital loop	Analog loop	not use not use
PIO bit(8):U/AN	0	1		
μ/A-->	μ	A		

The modem specifications are given below. This optional remote modem uses a modem IC in the ICRCVXXXACF series made by Rockwell. This IC is pin-compatible with 14.4 kbps and 28.8 kbps products. For this reason, the mo dem must be designed to accommodate 28.8 kbps products simply by changing the IC in order to satisfy the future requirements of the marketplace although the 14.4 kbps products with a low unit price will be used at the outset.

2. KX-TVS204

2-1. Overview

The KX-TVS204 (4DPITs card) with 4 ports is optionally mounted on the KX-TVS200 for DPITs interfacing only. It shares the same circuit board outline with the existing DSP card of the KX-TVS102. This enables the KX-TVS200 to share its slot cabinet with the KX-TVS100, and it also enables mixed mounting between the KX-TVS200 and KX-TVS102. Along with the single circuit board design, DSPIC masking and the creation of six circuit board layers have been implemented. The general configuration is shown in the illustration below.



The KX-TVS204 has a construction in which the existing KX-TVS102 DPITs interface sections are connected through a dual buffer system. Two DSP gate arrays and four mask DSP ICs are mounted as a result. Two ports are provided, and by using only high/low lines, DPITs communication for two channels is enabled using a single port, and communication for 4 channels is enabled using two ports.The host CPU must identify the previously mentioned slot addresses and card identification addresses for the KX-TVS204.

The function of the DSP Card is integrated in the Slave Controller (IC101) and DSP (IC109). These LSI devices include the functions mentioned below.

Slave Controller
- •FIFO to communicate between Microprocessor and DSP.
- •Voice Port Interface to transfer ADPCM data between system memory and DSP.
- •D-PITS interface to receive and send digital data by D-PITS protocol.
- •Line interface control I/O port to detect BELL, off-hook control, etc.

DSP (IC109)
- •Compression/extension of voice data by ADPCM algorithm.
- •To detect and generate DTMF.
- •To detect and generate TONE.
- •Detection of VOX (no-sound) condition. (To detect the condition of completed conversation.)
- •Automatic gain adjustment of recording level.

2-2. CPU Card Interface

Refer to section 1-10. Expansion Bus.

2-3. DSP Clock

4.096MHz provided from the CPU card is input to the DSP (IC109 - 53pin) as a basic clock.
This clock is input to the PLL inside DSP. PLL generates 14.336MHz(PLLCLK) from this clock. PLLCLK is divided into four inside and generates CLKOUT1 and CLKOUT2.
Figure 4 - 22 is standing of CLKOUT1 and indicates the third phase (Q3) is about to begin. Hereafter, phase no. Q1 - Q4 explains the bus operation.

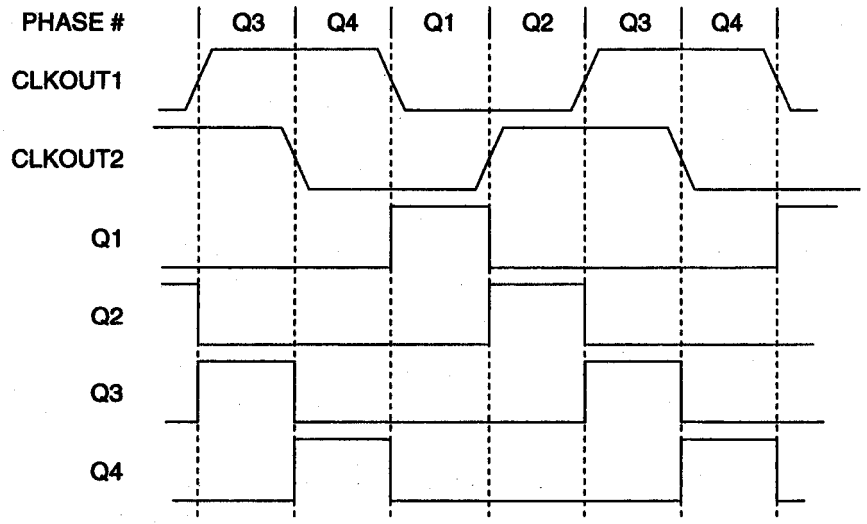


Fig. 4-24. DSP Clock

2-4. Parallel DSP Port

DSP installs control signals mentioned below to interface with Program ROM or a IC101 inside register.
- •16bit parallel data bus (A15 - A0)
- •16bit parallel data bus (D15 - D0)
- •Chip select (PS, DS)
- •Timing Control (STRB, R/WN)

(1) External read out cycle

The following are phenomena generated with the external read out cycle.

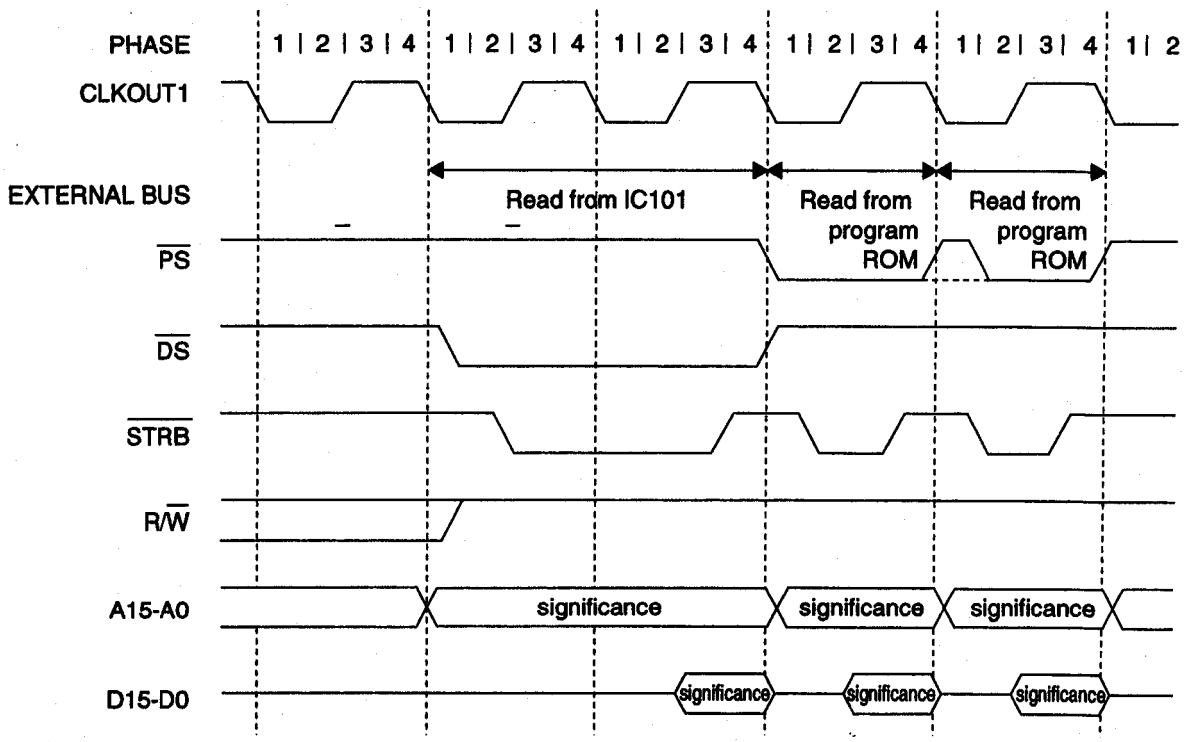
1) In the first phase (Q1), DSP starts driving address bus, and makes either PS or DS low level. To indicate the external memory's read out, R/W signal becomes high level.

2) At the beginning of the second phase (Q2), STRB signals indicating the effectiveness of the address bus output, and is used to generate a read enable signal with the R/W signal.

3) At the end of the third phase (Q3), data is taken in.

4) At the beginning of the fourth phase (Q4), the STRB signal is cancelled. PS, or DS signal and address bus are of no effect, and ends the external read out cycle.

Control signal PS, DS, STRB and R/W are generated only when the external memory location has gained access to. PS is asserted only when Program ROM (IC107/IC108) has gained access . DS is asserted only when the internal register of IC101 has gained access.



Timing 4-22. Read Cycle

(2) External write in cycle

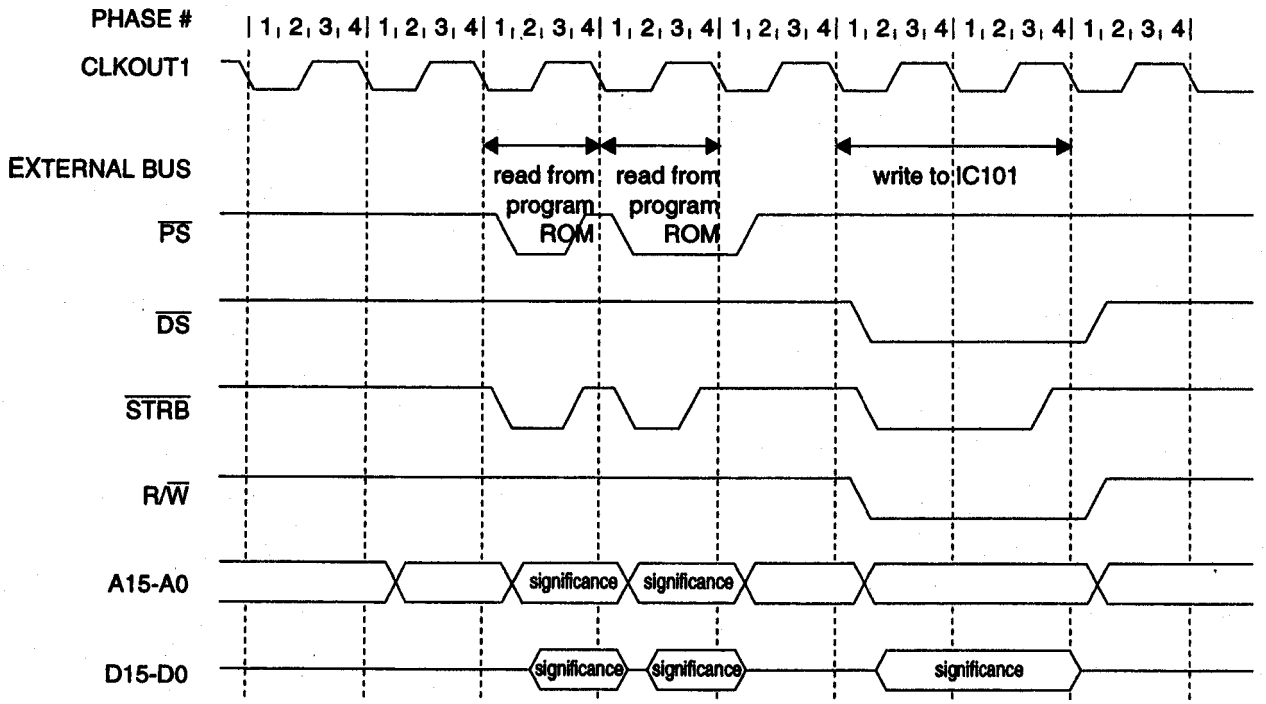
The following are phenomena generated with the external write in cycle.

1) In the first phase (Q1), DSP starts driving address bus, and makes DS active low. The R/W signal be comes low level for writing in external memory .

2) At the beginning of the second phase (Q2), the STRB signal indicates the effectiveness of the address bus output, and is used to generate read a enable signal with the R/W signal.

3) At the beginning of the second phase (Q3), data bus becomes active.

4) At the beginning of the fourth phase (Q4), the STRB signal is canceled. The Processor makes the address bus and DS signal invalid, and ends access of the external write in cycle.

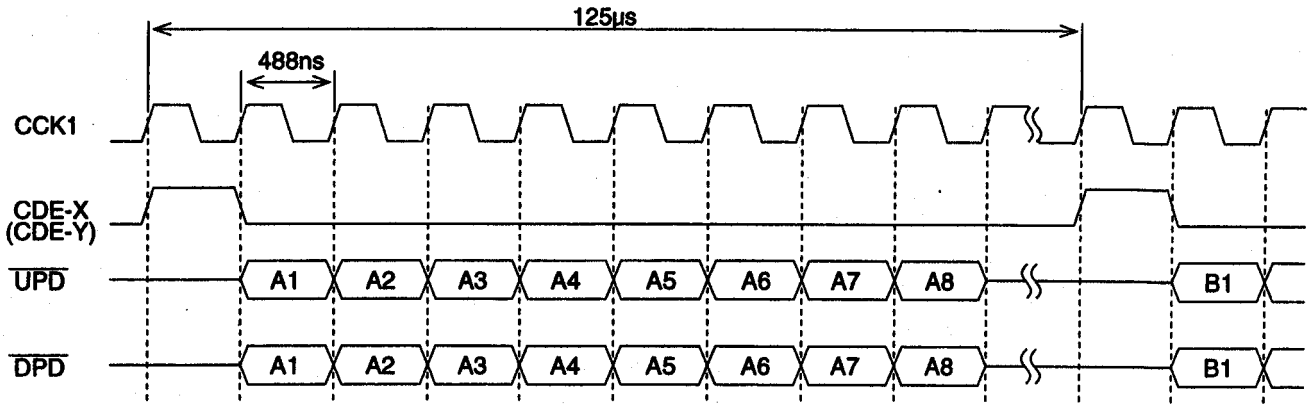


Timing 4-23. Write Cycle

2-5. DSP serial port

DSP serial port is used with the interface for the D-PITS B channel (Digital Voice Data).
This port is connects IC101 with CCK1, UPD, DPD, CDE-X(IC109A) and CDE-Y(IC109B) signals.
CCK1 is a 2.048MHz's serial shift in/out clock. UPD is 8bit PCM formatted voice data output from DSP. It is sent out to the PBX through D-PITS interface logic internal IC101. DPD is DSP input of PCM formatted voice data received from the PBX. CDE-X(CDE-Y) is an 8 KHz frame pulse input to enable to send or receive effective data of a serial port.

Serial Port Transfer Timing is shown in Timing 4-24.



2-6. D-PITS digital interface

D-PITS digital interface is provided with IC101. D-PITS interface built-in IC101 extracts effective data (2B + D) from a receiving D-PITS data stream, transfers D channel receiving data to voice port, and B channel receiving data (PCM Voice Data) to DSP. Sending out D-PITS data stream formed with D channel sending out data received from Voice Port and B channel sending out data received from DSP, is output to the COL card.
D-PITS interface is a digital interface, line bit rate : 512kBPS's, 2 line time share data format. Its communication format is 2B+D (B:64kBPS, D:16kBPS) and executes ping-pong communication every 8kHz (125us).

Data format B channel is 64kBPS u/A PCM format and D channel is 16kBPS HDLC format.

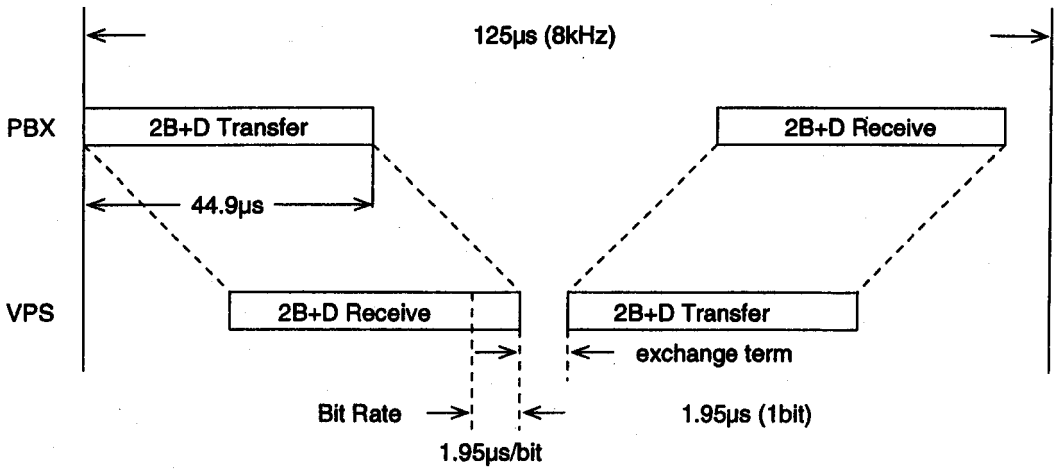
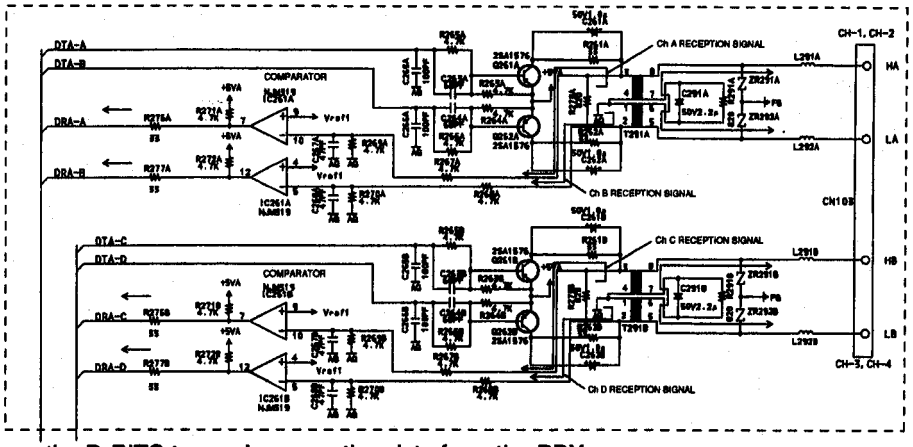


Fig. 4-25. D-PITS Data Transfer

Bit allotment of the DPITS frame is described below. S(1 - 5) is a zero pattern of 5 bits and is used as hardware to synchronize receiving and sending data with PLL.MA (1 - 3) is a 3-bit zero pattern data against AM1 symbolization and is used to detect the head of effective data. HK sends out an installed value inside the HK port. D(0 - 1) is 2 bit/frame HDLC data channel. B1 (7 - 0), B2 (7 - 0) are received and sent out in an 8-bit PCM data by MSB first individually.

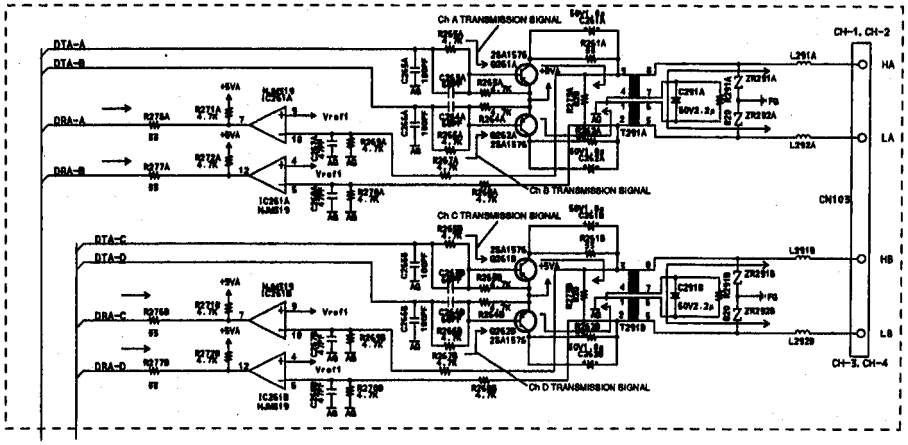
S1	S2	S3	S4	S5	MA1	MA2	MA3	HK	D0	D1	B17	B16	B15	B14	B13	B12	B11	B10	B27	B26	B25	B24	B23	B22	B21	B20	PRY
5					3				2		8								8								1

3-8. D-PITS Line Receiver



This logic allows the D-PITS to receive reception data from the PBX.
The D-PITS reception data flows through HA ↔ L291A ↔ T291A (8 - 7) ↔ C291A ↔ R291A ↔ T291A (6 - 5) ↔ L292 ↔ LA
HB ↔ L291B ↔ T291B(8 - 7) ↔ C291B ↔ T291A(6 - 5) ↔ L292B ↔ LB

3-9. D-PITS Line Transceiver



This logic allows the D-PITS to transmit transmission data to the PBX.
The D-PITS transmission signals flow as follows.

DTX - A = IC101A - 17 ↔ R113A ↔ R265A ↔ Base of Q261A.
DTX - B = IC101A - 18 ↔ R114A ↔ R266A ↔ Base of Q262A.

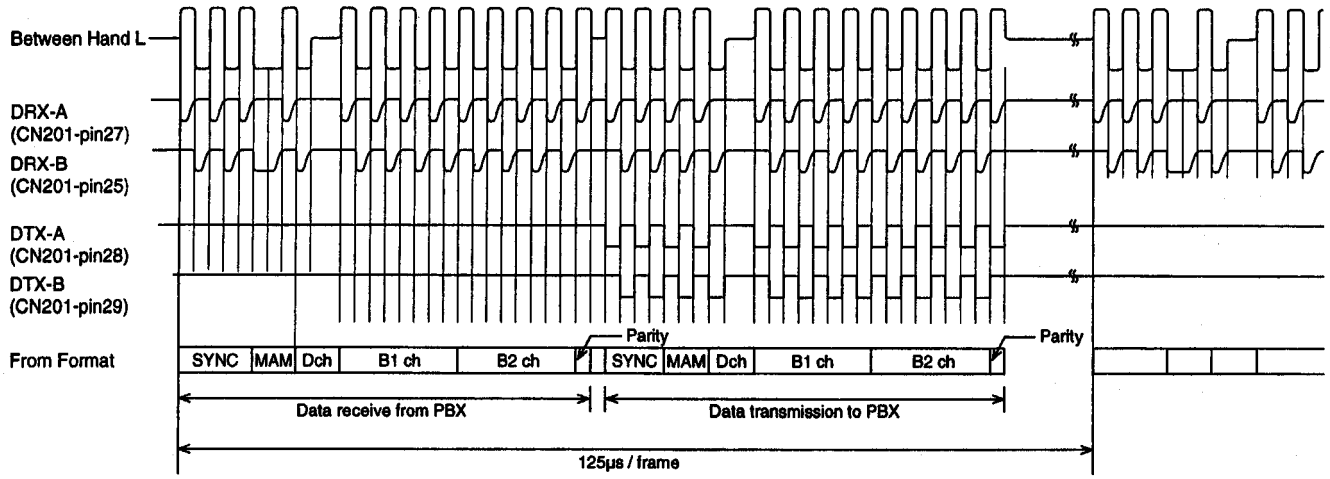
DTX - C = IC101C - 17 ↔ R113B ↔ R265B ↔ Base of Q261B.
DTX - D = IC101B - 18 ↔ R114B ↔ R266B ↔ Base of Q262B.

If IC101A drives DTX - A (DTX - B) to low level, Q261A (Q262A) is turned ON and the loop current flows through
If IC101B drives DTX - C (DTX - D) to low level, Q261B (Q262B) is turned ON and the loop current flows through as follows.

+5VA ↔ Q261A (E - C) ↔ C261A ↔ T291A (3 - 4) ↔ AG
+5VA ↔ Q262A (E - C) ↔ C262A ↔ T291A (2 - 1) ↔ AG

+5VA ↔ Q261B (E - C) ↔ C261B ↔ T291B(3 - 4) ↔ AG
+5VA ↔ Q262B (E - C) ↔ C262B ↔ T291B(2 - 1) ↔ AG

This loop current transition generates the D-PITS transmission data between T291A/T291B - pin 8 and T291A/T291B - pin 5.
As a result, T291A/T291B drives the HA/HB - LA/LB line corresponding with DTX-A/DTX-B.



Timing 4-28. D-PITS Transmission

4. POWER UNIT

4-1. Outline

Outline of power supply unit

The power supply unit on the KX-TVS200 is a multiple-input, separately excited switching power supply. Any AC input voltage from 115V to 240V is supported without the use of a selector switch. There are four secondary outputs: 12V for driving the hard disk drive motor, 5V with and 5V without instantaneous power failure backup for driving the logic system, and -5V for driving the interfaces.

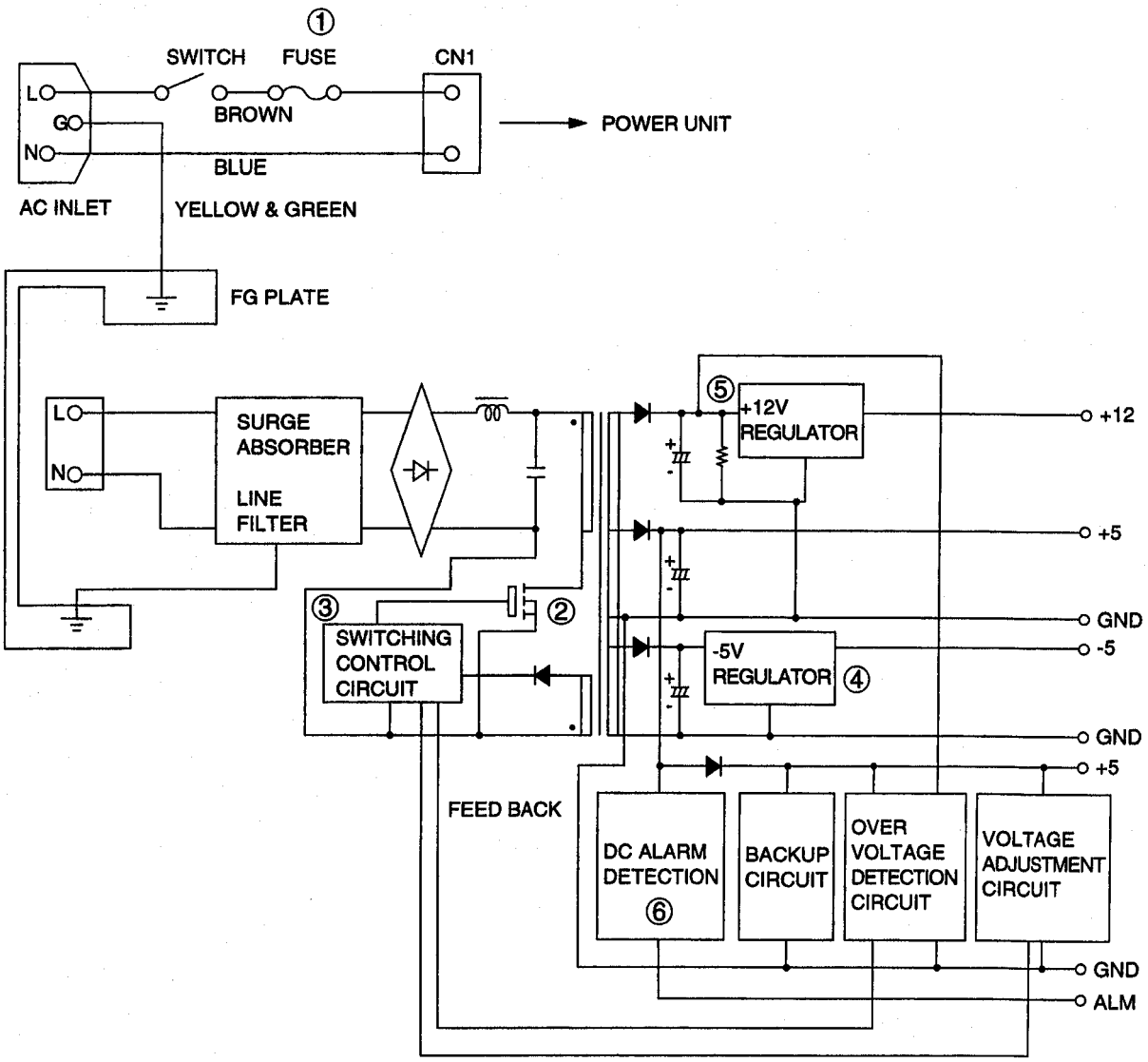
The unit's protection functions include the DC alarm detection function, overvoltage detection function, and overcurrent detection function.

Surge absorbers are provided between the lines and between the unit and ground at the primary side of the power supply circuit, and the immunity from surges is further improved by incorporating a gap type of absorber between the unit and ground. A transformer, which is designed to improve the harmonic characteristics and which complies with the IEC950 standard, is provided at the primary side. The electrolytic capacitor for primary side smoothing has a large capacity to provide back-up during instantaneous power failures, and it comes with a cover to prevent a fire from spreading in the event of trouble. A FET is used for primary side switching, and an AC/DC converter control IC is employed for its control section. This IC provides the overcurrent detection function, overvoltage detection function, and soft start function.

The secondary side circuitry of the power supply consists of three systems which deliver +12V, +5V and -5V through the power transformer. The +5V system is further divided into a +5V circuit with a backup function and a +5V circuit without a backup function. The +12V and -5V voltages are generated by using a 3-pin regulator to drop the rectified DC voltages supplied from the transformer. The overvoltage detection circuit monitors the +12V and +5V voltages of the secondary side circuit. The overcurrent detection circuit serves to narrow down the originating output when an overcurrent occurs in one of the secondary side systems. The +5V system with the backup function supplies power to the logic system circuit; the +5V system without the backup function supplies power only to the LED and RS-232C driver. The +5V system with the backup function uses a 4.7/3ÊF super capacitor to back up the logic system circuit when an instantaneous power failure occurs. It also takes action in an instantaneous power failure: as soon as the supply of power from the primary side to the secondary side is interrupted in response to the monitoring of the DC alarm detection circuit, a DC alarm signal is output from the power supply and input to the CPU port.

A block diagram of the unit and a description of its operation are presented below.

Block Diagram



Schematic diagram ..... Refer to page 125.

4-2. Circuit Operation

· Start/stop circuit section (start mechanism)

After the AC voltage is supplied to the section, the supply voltage has reached the startup voltage with the current from the starting resistor and the IC has started operating, the power MOSFET starts to be driven. This generates bias in the transformer, and the supply voltage is applied to the IC from the bias winding (point "a" in Fig. 1).

After the supply voltage has reached the startup voltage, a voltage is generated in the bias winding, and while an adequate supply voltage is supplied to the IC, the supply voltage of the IC is supplied by the capacitor (C12) which is connected to Vcc.

During this period (area "b" in Fig. 1), the supply voltage continues to drop, and if it drops below the stop voltage of the IC before an adequate supply voltage is supplied from the bias winding, the power cannot be started (status "c" in Fig. 1).

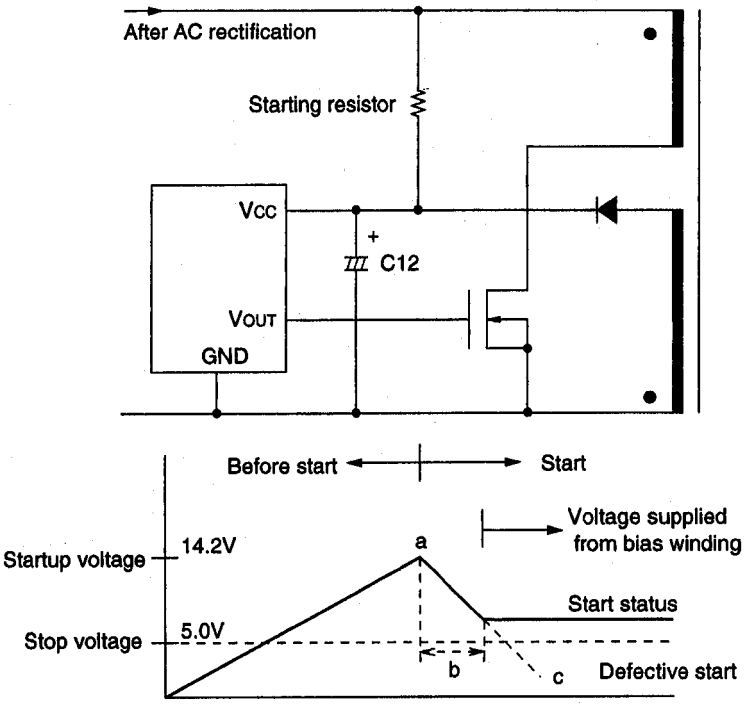


Fig. 1

Triangular wave oscillation:

Triangular waveforms are generated by a process of constant-current charging and constant-current discharging in the externally mounted capacitor which is connected to CT. The charging current to discharging current ratio is set internally, and the current value is determined by the externally mounted resistor which is connected to the RT pin. The RT pin voltage is determined at the level where the internal reference voltage (determined by the zener diode and npn transistor VEB, and temperature-compensated) has been divided by means of a resistor, and thus it is minimally affected by temperature variations or fluctuations.

· Over Voltage protection circuit

The power output has a self-diagnosis function which shuts down the power in order to protect the load in the event that a voltage which is abnormally higher than the normal output voltage is generated due to a failure in the control system, application of an abnormal voltage from an external source, or some other reason.(See Fig.2)

Basically, this function is set in such a way that the voltage at the Vcc supply voltage pin of the IC is monitored. However, since the Vcc voltage is normally supplied from the transformer drive winding and it is proportionate to the secondary side output voltage, the function is also activated when a secondary side output overvoltage occurs.

(1) If the voltage which is input to the OVP pin has exceeded the threshold voltage (6.0V typ.) as a result of a power output abnormality, the internal reference voltage of the IC is shut down, all control is suspended, and this stop sta tus is maintained.

(2) OVP is released (reset) under the following condition:

- The supply voltage must drop (Vcc < 8.4V typ.: OVP release supply voltage).

If supply voltage Vcc during OVP operation is stable at a value higher than the OVP release supply voltage (which depends on the starting resistor), OVP will not be reset unless the AC input is cut off. (See Fig. 3)

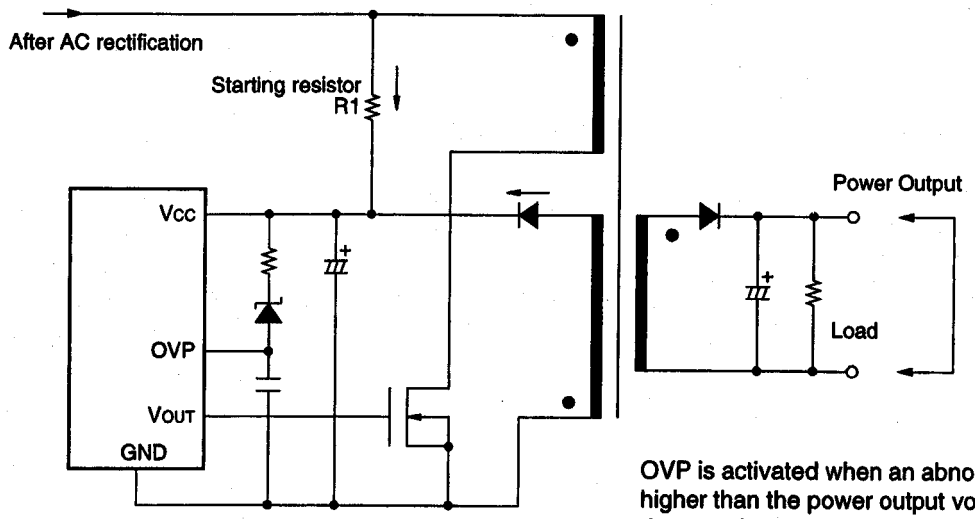
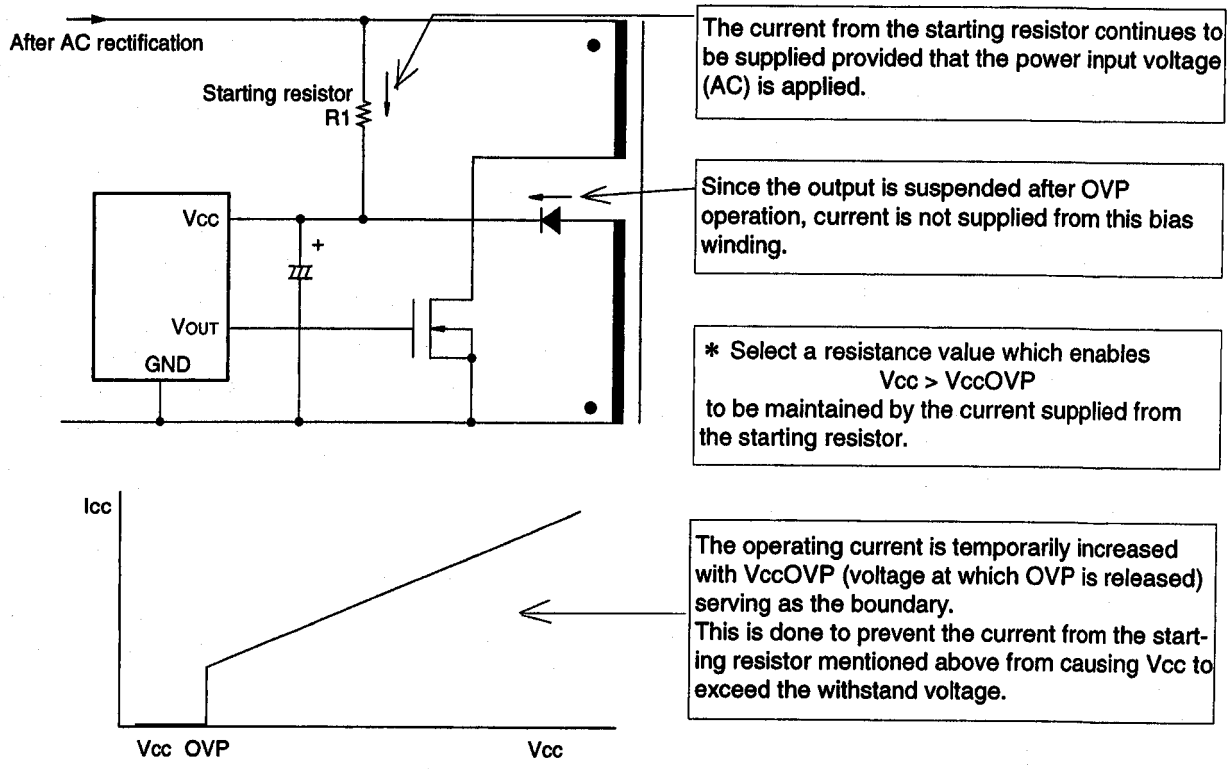


Fig. 2

OVP is activated when an abnormal voltage (which is higher than the power output voltage and which may damage the load) applied to the power output from an external source is detected by the primary side bias winding.



The current from the starting resistor continues to be supplied provided that the power input voltage (AC) is applied.

Since the output is suspended after OVP operation, current is not supplied from this bias winding.

* Select a resistance value which enables
Vcc > VccOVP
to be maintained by the current supplied from the starting resistor.

The operating current is temporarily increased with VccOVP (voltage at which OVP is released) serving as the boundary.
This is done to prevent the current from the starting resistor mentioned above from causing Vcc to exceed the withstand voltage.

Fig. 3

• Overcurrent protection circuit

By utilizing the fact that overcurrents in the power output are proportionate to the current flowing to the primary side main switch (power MOSFET), the pulse current flowing to the main switch is provided with a ceiling. In this manner, this circuit limits these overcurrents in the power output and protects the components susceptible to overcurrents.

The current flowing to the main switch is detected by connecting a low resistance between the power MOSFET source and power supply GND and monitoring the voltage at both ends of the resistor. Control is exercised in such a way that, when the power MOSFET is turned on and the threshold voltage of CLM (current limit) is detected, the output is turned off, the power MOSFET is turned off, thus preventing a current exceeding this limit from flowing. The threshold voltage of CLM is approximately -200 mV (typ.) at an ambient temperature of 25℃ in respect of GND of the IC. This control is repeated every cycle, and once an overcurrent is detected, the power MOSFET is kept in the OFF status for the rest of the cycle concerned, and it is not set on until the next cycle.

R4, R5 and C3 shown in Fig. 4 configure a filter circuit for filtering out the noise which is generated by the parasitic capacitance which is incidental in equivalent terms when the power MOSFET is turned on.

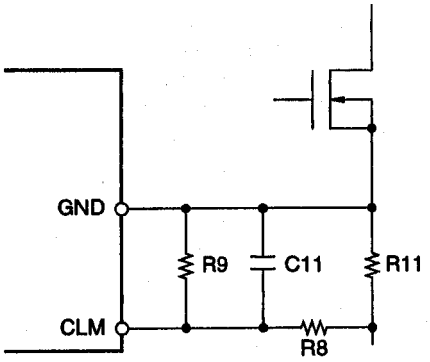


Fig. 4

- DC alarm operation

During normal operation, zener diode D401 is turned on (it turns on at 4.2V or above), Q401 is ON and, as a result, a high signal equivalent to the +5V power supply is output to the CPU port as the DC alarm signal. When the power from the primary side of the power supply is no longer supplied, the voltage at both ends of D401 interrupts the 4.2V voltage, and first D401 is set off. As a result of this, Q401 is set off, a low signal close to ground potential is output to the CPU port and the CPU proceeds with the action which it takes when an instantaneous power failure has occurred.

- Overvoltage detection circuit

The overvoltage detection circuit monitors the +12V and +5V voltages. In the case of the +12V voltage, the voltage before it is regulated to 12V is monitored, and when this voltage value exceeds 33V, D404 turns on, and the voltage is fed back to the primary side control IC via photocoupler PC2. Since the maximum input voltage of the +12V regulator IC is 35V, overvoltage detection is set to be activated at 33V, which is well within the 35V limit. In the case of the +5V voltage, when the output voltage or the voltage applied from an external source exceeds 6.2V, D405 turns on, and the voltage is fed back to the primary side control IC via photocoupler PC2.

- Voltage adjustment and feedback circuit

Shunt regulator IC103 is used for voltage adjustment and feedback. When the Vref voltage of IC103 is varied by varying VR101, the cathode voltage of the regulator is varied in proportion to the Vref voltage so that the current of photocoupler PC1 is controlled. As a result, the voltage of the +5V system can be adjusted. After the voltage has been adjusted, the shunt regulator operates in the same way as mentioned above in accordance with the voltage fluctuations in the +5V system to feed back a voltage which corresponds to the variation via the photocoupler to the primary side.

UTILITY COMMANDS

In this chapter, we explain commands which can be used by a general user.

In order to use, choose <Utility Command> in <System Administration Top Menu> of Administrator Service. Command waiting prompt is on the screen. (See below.)

(Type "Kme" and enter password "Panasonic" to use all commands.)

```
$
```

Input command after "$".

```
$ command
```

(Type "Kme" and enter password "Panasonic" to use all commands.)

1. HELP COMMAND (HELP)

(1) Function

To show the list which can be used in the VPS.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$HELP
    ONLN            : System Online
    OFLN            : System Offline
    PASS            : Password setting
    TIME            : Time & Date setting
    PSET            : Report Print Out Time setting
    ELOG            : Device Error Log Listing
    SAVE            : VPS Program & Data Save (VPS -> PC : Xmodem)
    LOAD            : VPS Program & Data Load (VPS <- PC : Xmodem)
    GPRN            : Parameter Global Printing
                      ( only 'ASCII Terminal' mode )
    VERS            : Program Version Check
    QSET            : Quick Setup
    MWL             : MWL Retry count Set (1-3)
    MRL             : Minimum Recording Length Set (0-3)
    MPLT [opt]      : Registered User Prompt No. List
                      [opt] : 1     -->  User Prompt 1
                              2     -->  User Prompt 2
                              None  -->  User Prompt 1&2
    CREP [no]       : Custom Menu Information List
                      [no]  : Custom Menu No. (1-100)
    CCLR [no]       : Custom Menu Access Counter Clear
                      [no]  : Custom Menu No. (1-100/0) (0:Clear All)

    LMON            : Line Monitor
    RUTD            : DTNF Information Display

    (the following are displayed only for privileged managers)

    DCLR [drv], [opt] : Initialize parameters and Data
                        [drv] 1 or 2
                        [opt] 0 : All Parameters and Voice Data
                              3 : All Parameters and Voice Data
                                  except Usr Prompts
                              4 : Only Usr Prompts
    DCPY            : Disk       Copy DISK1 => DISK2
    PCPY            : Program    Copy DISK1 => DISK2
    GCPY            : Guidance   Copy DISK1 => DISK2
    XCPY [opt]      : Program, System Guidance Copy DISK2 => DISK1
                      [opt] None : Program & System guidance
                            1    : Program
                            2    : System Guidance
                            3    : User Prompts
    SYSD            : System Disk Set Up (DISK2)
```

2. ONLN Command (on line service control)

(1) Function

VPS service is resumed.

Please refer to < 1.2 OFLN command> for OFLN command.

(2) Operand

Nothing.

(3) How to use, example for usage

a) When throwing normal on line command

```
$ONLN
 **    ON LINE MODE   **
```

b) Below mentioned cases don't become on line condition.

- In the D-PITS interface, D-PITS communication circuit is not connected. Or Communication circuit connected the install on PBX side is not shared as VM port in DPITS interface.
- There is no DSP/CO card.

```
$ONLN
 **    OFF LINE MODE   **
```

3. OFLN COMMAND

(1) Function

To break VPS service.

VPS service is suspended.

(2) Operand

Nothing.

(3) How to use, example for usage

a) When throwing command, VPS service is not used.

```
$OFLN
 **    OFF LINE MODE   **
```

' Becomes off line service immediately.

b) When throwing command, VPS service is used.

```
$OFLN
 ***    Now Line is used !!   *** < WAIT >
```

' The execution of this command is in the waiting condition, when service usage finishes, the command is executed.

```
** OFF LINE MODE **
```

4. PASS COMMAND (Install password)

(1) Function

To install and cancel administrator and system passwords.

An Administrator password is the password to enter from the initial screen to the terminal select screen.

A System reset/clear password is the password to be asked when reset is executing on the <System Reset/Clear> screen.

Without a password, installation is possible in both cases.

The Password should be one word with less than 8 letters or numbers, or special symbols (underline, period, space).

(2) Operand

Nothing.

(3) How to use, example for usage

```
$PASS
 1 : Administrator Password  2 : System Reset/Clear Password : =
```

① In the of case new registration

Select 1 or 2.

```
$NEW PASSWORD : =
```

Input password.

```
$VERIFICATION : =
```

To confirm password, input password again.
When it is different from the first one, start from <New Password> again.

Note: Input password is not shown on the screen.

② Change

Select 1 or 2.

```
$OLD PASSWORD : =
```

Input present registered password.

```
$NEW PASSWORD : =
```

Input new password.

```
$VERIFICATION : =
```

To confirm input password, input the password again.

Note: When it is an administrator password, <present password> is not required.

③ Password cancellation

Select 1 or 2.

```
$OLD PASSWORD : =
```

Input present registered password.

```
$NEW PASSWORD : =
```

Press return key without inputting anything.

```
$VERIFICATION : =
```

Press return key without inputting anything.

5. TIME COMMAND (Installation of Time/Date)

(1) Function

To install time and date.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$TIME
  Current time is 12 : 34, PM
  Enter new time  ( hh : mm, AM/PM ) : =
```

Input current time.

Example: In the case of 2:56 PM.

Enter new time (hh:mm, AM/PM) : = 2:56, PM

```
Current date is 29-JAN-'93
Enter new date  ( DD-MM-YY ) : =
```

Input current date (Date - Month - Year) (Input last two figures for year)

example: In the case of July 13th. 1973

Enter new date (DD - MM - YY) : = 13-7-73

Note: Input time and date correctly, because VPS service owes much of its work to time and date. Following are also changed with the change of time and date. Notification of arrival, Message auto distribution send, Designated time between mail boxes message distribution send, Auto transfer function, etc.

6. PSET COMMAND (Install report printing out time)

(1) Function

This command makes it possible to print out reports at a certain time.

The Following reports are printed out.

①Disk Usage Report

②Port Usage Report

③Call Account data Report

(2) Operand

Nothing.

(3) How to use, example for usage

```
$PSET
  Report Print Out Service  [ Disable ]
    1 : Enable  2 : Disable : =
```

Input 1 for install, input 2 for cancellation.

When you input 1, still more install the time for printing out.

```
Enter The Print Out Time  ( hh : mm, AM/PM ) : =
```

Example: In the case of 2:56 PM

Enter the Print Out Time (hh:mm, AM/PM) : = 2:56, PM

7. ELOG COMMAND (Display device error)

(1) Function

To display the error trace of the DSP card, MAIN card, Hard disk, etc.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$ELOG
        DEVICE      ERROR                TIME
        -----       -----                -----
  1.    CPU         MEM-GET              14-JUL 14:00 PM
  2.    CLOCK                            15-JUL 12:40 AM
  3.    DISK        DATA R/W (xx/yyyy)   15-JUL 13:02 PM
  4.    DSP1        SCAN                 15-JUL 13:02 PM
  5.    DSP4        FIFO                 15-JUL 13:15 PM
  6.    CPU         APPLICATION (2)      15-JUL 13:16 PM
```

[Explanation]

- The following examples of errors.

CPU	MEM - GET	CPU card impossible to acquire memory.
	APPLICATION (n)	Application error occurred momentarily while working.
CLOCK		Hindrance occurred in clock IC.
DISK	DATA R/W (XX:YYYY)	R/W error in hard disk. (master) XX : error code YY : error sector No.
DSPn	SCAN	DSP Card n is not equipped. CPU cannot confirm the DSP card.
	FIFO	DSP or FIFO error occurred momentarily while working.

Note: n Card No. 1 ~ 4

- After displaying the error contents, it asks whether to clear the error trace data or not.

```
Clear ? ( Y/N ) : =
```

You can clear the error trace data by inputting "Y".

8. SAVE COMMAND (Program/Data Back up)

(1) Function

To back up a certain program or data on the VPS hard disk.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$SAVE
      Disk Data Down-load ( Xmodem )
            1 : Program
            2 : Parameters
            3 : System Prompts
            4 : User Prompts-1
            5 : User Prompts-2
            6 : Custom Service Menu
            7 : Personal Greeting
            8 : Company Greeting
 Select No. : =
```

Select the item to be backed up.

```
To start press 'RETURN'
```

Press the return key.

```
Start _ _ _ _ _ Download !!
```

To select the data receiving mode (Xmodem) in DTP, point to the name of the file to be backed up. Now it is possible to transfer the data by Xmodem protocol.

Note:

① Command cancellation before transfer ' '¥' or '＼'

② Transfer cancellation during receiving ' follow your communication software.

Note: Please refer to another sheet for the details of SAVE command.

9. LOAD COMMAND (Program/Data up-date)

(1) Function

To update a certain program or data on the VPS hard disk.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$LOAD
      Disk Data Up-load ( Xmodem )
            1 : Program
            2 : Parameters
            3 : System Prompts
            4 : User Prompts-1
            5 : User Prompts-2
            6 : Custom Service Menu
            7 : Personal Greeting
            8 : Company Greeting
 Select No. : =
```

Select the item to update.

```
To start press 'RETURN'
```

Press the return key.

```
Start _ _ _ _ _ Upload !!
```

To select the data receiving mode (Xmodem) in DTP, point to the name of the file for update. Now it is possible to transfer data by Xmodem protocol.

Note:

① Command cancellation before transfer ' '¥' or ' \ '

② Transfer cancellation during receiving ' follow your communication soft.

Note: Please refer to another sheet for the details of LOAD command.

10. VERS COMMAND (To display each card and program version of hard disk)

(1) Function

To display CPU ROM and the program version on the hard disk.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$VERS

 V.P.S. PROGRAM VERSION

   MAIN DISK  :  VC2100 (1.00)  ..... ①
   MAIN ROM   :  VC11A  (1.00)  ..... ②
```

[Explanation]

① Hard disk • program version display

MAIN DISK : Version (Internal version)

Note: Users do not need to pay attention to <Internal version> .

② CPU ROM • program version display

MAIN ROM : Version (Internal version)

11. QSET COMMAND (Quick Setup)

(1) Function

To start Quick Setup.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$QSET

Thereafter, Quick Setup Menu starts.
```

12. MWL COMMAND (To install the number of Message Waiting lamp retry)

(1) Function

In case the message waiting lamp turn fails to on and off, VPS retries after a certain period.
With this command the number of retries can be installed.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$MWL
 Current Setting of M.W.L. Retry Count is 3
 Enter M.W.L. Retry Count (1-3) : =
```

' Select the number of retry (1 ~ 3 times)

13. MRL COMMAND (To install the minimum time of message recording)

(1) Function

With this command, the minimum time of message recording can be installed. A message shorter than installed here doesn't seem to be a message, so not be recorded.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$MWL
 Current Setting of Minimum Recording length is 3
 Enter Minimum Recording length (0-3) : =
```

' Input the recording time by seconds (range: 0 ~ 3 seconds)
To input 0 seconds means all recorded messages are effective.

14. MPLT COMMAND (Display registered user prompt)

(1) Function

To display prompt No. of registered (recorded) user prompt

(2) Operand

Nothing.

```
$MPLT
```

(3) How to use, example for usage

```
$MPLT
***** List of Registered User Prompt 1 No. ( [1], [2], . . . , [619] ) *****

  1,   2,   3,   4,   5,   6,   7,   8,   9,  10,  11,  12,  13,  ...
 21,  22,  23,  24,  25,  26,  27,  28,  29,  30,  31,  32,  33,  ...
 41,  42,  43,  44,  45,  46,  47,  48,  49,  50,  51,  52,  53,  ...
 61,  62,  63,  64,  65,  66,  67,  68,  69,  70,  71,  72,  73,  ...
 81,  82,  83,  84,  85,  86,  87,  88,  89,  90,  91,  92,  93,  ...
101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113,  ...
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...

Total Number Registered = 419                              ..... ①

***** List of Registered User Prompt 2 No. ( [1], [2], . . . , [619] ) *****

  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,  ...

Total Number Registered = 0                                ..... ②
```

[Explanation]

① The total number of registered User Prompt 1.

② The total number of registered User Prompt 2.

15. CREP COMMAND (Display custom menu information)

(1) Function

To display installed information inside the designated number' custom menu.

In case the custom menu is nested, it is displayed in stages (maximum of 8).

(2) Operand

It is possible to select from 1 to 100 with the custom menu number display.

(3) How to use, example for usage

```
$ crep 20
Custom  [ 20]   ( User-1 ) ( Access :   0 ) ( Menu Msg. : None )
                    ↓           ↓           ↓           ↓
          (Remarks 1)  (Remarks 2)  (Remarks 3)  (Remarks 4)
 |  < Custom Service Entry Menu > → (Remarks 5)

[1]-Xfer Mbx (401)          → (Remarks 6)

[2]-Xfer Extn (402)         → (Remarks 7)

[3]-Custom [ 21] (System) (Access :   0) (Menu Msg. : None)
 |      |  < Voice Mail Information Eng. >
 |     [1] – Custom [ 22] (User-2) (Access :   0) (Menu Msg. : None)
 |      |      |  < Voice Mail Information Eng. >
 |      |      [1]- Operator
 |      |      [2]- Name Dial
 |      |      [3]- Subscriber
 |      |      [4]- Dprt Dial
 |      |      [*]- Main Menu
 |     [*]-Main Menu
[6]- Operator
[7]- Exit
[8]- Pre. Menu
[*]- Main Menu
[#]- Exit
$
```

Note:

Remarks 1) Custom menu No.

Remarks 2) Prompt kind (System / Use - 1 / User - 2)

Remarks 3) Custom service access number

(How many times this custom menu is accessed by telephone service.)

Remarks 4) The condition of menu message recording (Rec / None)

Remarks 5) Description

Remarks 6) Mail box number

Remarks 7) Extension number

16. CCLR COMMAND (To clear custom menu access number)

(1) Function

To clear a selected number of custom menu access number.(The number of times custom service number was accessed by telephone service.)

(2) Operand

It is possible to select from 1 to 100 with the custom menu number to clear.

When 0 is selected, all of the custom menu is cleared.

(3) How to use, example for usage

```
$ CCLR 20
  Custom Menu < 20 >  Accessing Counter is Cleared

$ CCLR 0
  All Custom Menu Accessing Counters are Cleared
```

17. DCLR COMMAND (Initialize parameter, data of hard disk)

(1) Function

To clear the parameter or data of the selected drive's hard disk.

The following is to be cleared.

- Each parameter (Mail box information, report information, etc.)
- Voice data (system guidance, user guidance, message, etc.)

After execution, VPS should start up again.

(2) Operand

```
$DCLR [drv] [opt]
```

① [drv]

Select drive No.

1 : Drive 1

2 : Drive 2

② [opt] (Option)

Select the parameter and data to be cleared.

0 : Install hard disk to system disk, then clear all parameters and voice data.

3 : Install hard disk to system disk, then all parameters and voice data, except for user guidance.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) ①

4 : Clear all voice data except for user guidance.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) ①

5 : Clear user guide only.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) ①

(3) How to use, example for usage

Example is shown blow.

```
$DCLR 1, 0                    ..... ①
  Please POWER OFF !          ..... ②
$DCLR 2, 3                    ..... ③
  Please POWER OFF !
$DCLR 1, 4                    ..... ④
  Please POWER OFF !
```

[Explanation]

①To clear all parameters and voice data in drive 1.

②To display the message urges to start up VPS again.
It won't accept key input at all. Turn the power off and then on.

③To clear all voice data except user prompt in drive 2.

④To clear all user prompts in drive 1 and user prompt 2.

18. DCPY COMMAND (All selector copies between drives)

(1) Function

To copy the data (all sector) in drive No. 1 to drive No. 2.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$DCPY
  001234                      ..... ①
$                             ..... ②
```

[Explanation]

①To display the sector number of present copying.

②To display command prompt "$".
It means copy finishes normally.

Note:

When an error caused by the hard disk occurs during execution of DCPY, the error sector number is displayed. The sector is skipped, then disposition continues. It is recommended to check the sector with the RECO command and execute recover after DCPY finishes. Concerning the RECO command, please refer to <Chapter 8 8.7 RECO command>.

The following are the commands displayed during error sector copying.

- DCPY
- PCPY
- GCPY
- XCPY
- SYSD

19. PCPY COMMAND (Program copy between drives)

(1) Function

To copy the VPS program in drive No.1 to the program region of drive No.2.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$PCPY
 001234                    ..... ①
$                          ..... ②
```

[Explanation]

①Sector number presently copying.

②To display Command prompt "$".

20. GCPY COMMAND (System guidance copy between drives)

(1) Function

To copy system guidance in drive No.1 to drive No.2.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$GCPY
 001234                    ..... ①
$                          ..... ②
```

[Explanation]

①Sector number under presently copying.

②To display Command prompt "$".

21. XCPY COMMAND (Copy from drive No. 2 to drive No. 1)

(1) Function

To copy from drive No.2 to drive No. 1. The following are copy objects.

①Program

②System guidance

③User prompt

(2) Operand

```
$XCPY [para]
```

①[para]

Nothing	: Program, System guidance copy	(Drive 2 ' Drive 1)
1	: Program copy	(Drive 2 ' Drive 1)
2	: System guidance copy	(Drive 2 ' Drive 1)
3	: User prompt copy	(Drive 2 ' Drive 1)

(3) How to use, example for usage

```
$XCPY                                                    ..... ①
  001234                                                 ..... ②
$                                                        ..... ③
$XCPY 3                                                  ..... ④
  XCPY (User-Prompt Copy Disk2 -> Disk1)  Start !        ..... ⑤
  001234
  XCPY (User-Prompt Copy Disk2 -> Disk1)  End !          ..... ⑥
    *** Total Copy Number : 125***                       ..... ⑦
$
```

[Explanation]

①To copy program and system guidance.

②To display sector number presently copying.

③To display command prompt "$".
Copy ends normally.

④To copy user prompt.

⑤To display copy starts.

⑥To display copy ends.

⑦To display the user prompt's total number copies.

22. SYSD COMMAND (Install Drive 2 to system disk)

(1) Function

The Following jobs are required to install Drive No.2 to a system disk.

①To initialize Drive 2. (FORMAT 2)

②To clear Drive 2. (DCLR 2, 0)

③To copy program from Drive 1 to Drive 2.

To copy system guidance from Drive 1 to Drive 2.

To copy user prompt from Drive 1 to Drive 2.

During this operation you can choose to copy-only user prompt 1 or only user prompt 2 or both user prompt 1 and 2. (To put coming up prompt No. in order, then store in Drive 2.)

(2) Operand

Nothing.

(3) How to use, example for usage

```
$SYSD
  Select User Prompt No. ( 0-2, 9 )
    Ex.      If you select No. 1,

             Only User Prompt 1 is copied from Disk1 to Disk2.

                0 :  User-1 & User-2
                1 :  User-1
                2 :  User-2
                9 :  Not Copy User Prompt  =>  2
                The record time will be set to 32 hours.
                Are you sure?[Y/N]=Y

  *** FORMAT  ***                                        ..... ①
  *** DCLR    ***                                        ..... ②
    ****************
  *** COPY    ***                                        ..... ③
      0005A0
      0020a0
  *** USRP COPY* * *                                     ..... ④

$                                                        ..... ⑤
```

[Explanation]

①Disk 2 format.

②To initialize disk 2. (To initialize each table information)
To be displayed every time each table is initialized.

③To copy program/ system guidance.
Sector No. copying at present is displayed in real time.

④User prompt's copy.

⑤To display command prompt "$".
Copy finishes normally.

23. LMON COMMAND (Circuit condition display)

(1) Function

To display the circuit condition every 1.5 seconds on the screen. Input \ to terminate display. In the case of an ASCII screen, it is displayed only once.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$ LMON
  Co No.    : Status
              1 : Ready
              2 : Ready
              3 : Error/Not Exist
              4 : Error/Not Exist
              5 : Error/Not Exist
              6 : Error/Not Exist
              7 : Error/Not Exist
              8 : Error/Not Exist
              9 : Error/Not Exist
             10: Error/Not Exist
             11: Error/Not Exist
             12: Error/Not Exist
```

Note:

"Ready"	••• Possible to serve
"Incoming Call Service"	••• Processing arrival service
"Outgoing call Service"	••• Processing sending service
"DSP Reset Processing"	••• Processing DSP reset disposition
"PITS Connect Processing"	••• Processing PITS connect disposition
"Error/Not Exist"	••• DPS Card is not loaded.

24. PUTD (DTMF Information Display)

(1) function

Used to display DTMF tones the VPS is receiving and sending.

Inaddition to DTMF, the following information is displayed.

A type of Incoming Call Service (Voice Mail, Automated Attendant, Custom Interview) when the caller enters any service.

One "✳" means 4 secs while VPS is recording message etc.

(2) Operand

See (3)

(3) How to use, the example of usage

Once you enter "PUTD", this mode is kept until you enter "PUTD" again.

Default setting of this mode for all ports is "OFF".

```
$ PUTD
        Target Port : ✳ ✳ ✳ ✳  ✳ ✳ ✳ ✳  ✳ ✳ ✳ ✳
$
```

If you want to change the mode back to "OFF", enter "PUTD" again.

```
$ PUTD
Target Port : 0000 0000 0000
Don't leave enabled after troubleshooting.
$

Note : "✳" means "enable" for the port
       "0" means "disable" for the port
```

If you want to set the mode for only one specified port, type "PUTD" and the port number.

```
$ PUTD
Target Port : 0000 0000 0000 ✳
Don't leave enabled after troubleshooting.
$                                ↑
                               port 1
```

Sample of display is as follows.

```
$PUTD
Target Port for Debug :
$

                                    * * * *  * * * * *  * * * *
[1] DTMF : #
[1] DTMF : 8
[1] A.Attend
[1] DTMF : #
[1] DTMF : 6
[1] Voice Mail
[1] DTMF : 1
[1] DTMF : 0
[1] DTMF : 1
[1] NonSub Svc
[1]
[1] DTMF : D
[1] DTMF : D
[1] Thank you
```

Warning

1. "PUTD" is a command originally used for troubleshooting. Do not use in normal use.
2. While "PUTD" mode is "ON", do not remove the RS-232C connection be cause the VPS is continuously sending data to the terminal, and it nay cause data overflow.

25. EMDM COMMAND (External modem setup)

(1) Function

Used to specify modem commands you want to send to external modem connected with VPS.

(2) Operand

Nothing

(3) How to use, the example of usage

You can set up to 5 AT commands and comment (information) for each command.

```
$ EMDM
Current AT Commands for External Modem is as follows.
  Nothing
Please enter command number you want to change.
   If you want to initialize all data, enter 0  : =1
===== Command No. 1 =====
Enter Comment  (Max:  32 Characters)  => TEST              ← Comment
Enter Command  (Max:  60 Characters)  => ATQ1&K0S0 = 1  ← Modem Command
Current AT Commands for External Modem is as follows.
  No. 1  Comment : TEST
         Command : ATQ1&K0S0=1
Please enter command number you want to change.
   If you want to initialize all data, enter 0 : =
     To send the AT commands,
       1. Connect Modem and VPS using RS-232C Straight Cable
       2. Access System Manager Service
            and press 9 + Command No. during the Top Menu
             Ex. *999 + 91 (to send Command No. 1)
```

• Modem Command Example
ATE0Q1&D0&S0 = 1&K0&Q0%C0
E0 : Commands are not echoed
Q1 : Disable responses to PC
&D0 : Ignore DTR signal
&S0=1 : DSR always ON (auto answer ON)
&K0 : Disables flow control
&Q0 : Select direct asynchronous mode
%C0 : Data compression disable

The modem commands for connecting with VPS vary with the modem maker.
Please check the manual of the modem.

★How to send the Modem Command to external modem
Please connect RS-232C straight cable between VPS and modem.
Note: You have to turn "PUTD" mode back to "OFF"
if you already set the mode "ON" for trouble shooting.
To send the command, please access System Manager Service,
and enter 9 + No. during the top menu.
For example, *999 + 91 (← VPS sends AT Command No.1).
After sending AT Command, VPS beeps out for about 2 sec.

MAINTENANCE AND TROUBLESHOOTING

1. SELF DIAGNOSTICS

The VPS executes self diagnostics when power up is executed. The power indicator informs the system conditions and the results of the diagnostics as shown in Table 5-1.

1-1. Normal Bootup

As the result of Self Diagnostics, if there is no problem in the VPS system, the operation mode follows the sequence 1 ' 2 ' 3 ' 4 as shown in Table 5 - 1.

1-2. Hardware Error Detection

When VPS detects an abnormal condition in the hardware by Self Diagnostics, VPS executes a Blinking sequence as shown in Table 5 - 2. In this operation VPS repeats only the Blinking sequence (VPS Service is cut off). Turn off the power source, find the cause of the error, and turn on the power source again.

1-3. Warning Error Detection

When connecting with a PBX by a D-PITS line, and there is no problem with the Self Diagnostics sequence, but modular connector to connect with PBX is pulled out, the VPS should maintain the Warning condition in the sequence 1 ' 2 ' 3 ' 4 as shown in Table 5 - 1. When Connecting the VPS to a programmed D-PITS port, the VPS is restored to operation mode from warning mode except when VPS does not have special obstacles.

1-4. Fatal Error Detection

As the result of System Initialization, when VPS detects an error as described below, Fatal Error is indicated in the sequence 1 ' 2 ' 3 ' 4 as shown in Table 5 - 1. When VPS falls in the error condition, If stops service. Turn off the power source , find the cause of the error, then turn on the power source again.

Facts of Fatal Error
- DSP/COL card module is not installed.
  Microprocessor cannot gain access to DSP/COL card module.
- Data access from the hard disk drive has failed.
- Time data access from the real time clock IC has failed.

Table 5-1. The Power Indicator Blinking sequence when Power Up System Initializes.

VPS System Conditions	Data Terminal Screen	Blinking Sequence of the Power Indicator
1. Power Up		Light ON
2. Diagnostics	CARD TEST	Light ON
3. Initialize	SYSTEM SETUP 1... 2... 3...	Blinking Repeat 0.25 sec ON and 0.25 sec OFF
4. Operation Mode	** ON LINE MODE **	Light ON
5. Warning Error	** OFF LINE MODE **	Blinking Repeat 0.5 sec ON and 0.5 sec OFF
6. Fatal Error	** OFF LINE MODE **	Blinking Repeat 0.5 sec ON and 3.5 sec OFF

Table 5-2. Power Indicator Blinking sequence when Power Up Self Diagnostics.

Error Type	Data Terminal Screen	Blinking Sequence of the Power Indicator Check: The blinking interval is 6 sec.
1. RAM Error	RAM R/W ERROR !! IC30x Adr [xxxxxx]···	The indicator blinks 2 times.
2. ROM Error	ROM ERROR :Sum Error!!	The indicator blinks 3 times.
3. HDD Error (case–1)	DISK ERROR :Initialize Error!!	The indicator blinks 4 times.
4. HDD Error (case–2)	DISK ERROR :No System!!	The indicator blinks 5 times.
5. HDD Error (case–3)	DISK ERROR :Program Load Error!!	The indicator blinks 6 times.
6. HDD Error (case–4)	DISK ERROR :Program Sum Error!!	The indicator blinks 7 times.

2. THE ERROR RESULTS OF THE SELF DIAGNOSTICS

2-1. RAM Error

The Microprocessor gains access to system memory (IC304/IC305/IC307/IC309) on the CPU card in sequence of write after read. When VPS detects a different written value from read value, it judges RAM Error. This examination is executed to all addresses of system memory, VPS shows the wrong address and data on system memory detected as follows:

RAM R/W ERROR !!IC30 Adr[error address]
WtData[write(correct)pattern] RdData[read(error)pattern]

Descriptions : $IC30_x$

This indicates the parts number of the error memory.
It is either IC304 or IC305 or IC307 or IC309.

Adr[error address]
This informs the error address in the system memory.
[Error address] is shown by 8-bit code.

WtData[write(correct)pattern]
This is a correct pattern which is written into the system memory by the Microprocessor. The type of write patterns are 0, 5, A or F.

RdData[read(error)pattern]
This is an error pattern which is read from system memory.

2-2. ROM Error

The Microprocessor reads all data from system ROM (IC306/IC307) on a CPU card by a 16-bit unit, then calculates the total of the data value. VPS judges error when the sum total differs from the correct value calculated beforehand.

2-3. HDD Error

These Errors are displayed when data transfer between the Microprocessor and hard disk drive fails. HDD Error has four messages depending on the error situation.

case - 1 : DISK ERROR : Initialize Error!!
This error indicates the Microprocessor detects an abnormal status of the hard disk drive.
Generally, this happens when the hard disk connecting cable is pulled out.

case - 2 : DISK ERROR : No system!!
This error indicates system program is not installed to the hard disk drive.
System program should be installed to the hard disk again.

case - 3 : DISK ERROR : Program Load Error!!
This error indicates system program installed in the hard disk failed in the process of being loaded to system memory. Most likely in the process of data transfer from the hard disk drive.
Generally digital logic inside the hard disk drive is out of order.
In this case, replacement of the hard disk drive is necessary.

case - 4 : DISK ERROR : Program Sum Error!!
The Microprocessor reads all system programs from the hard disk to system memory by a 32-bit unit. Then it calculates the total of the data value. VPS judges Program Sum Error when the total sum differs from the correct value calculated beforehand.
Generally, media inside the hard disk drive is out of order.
In this case, replacement of the hard disk drive is necessary.

3. ERROR LOG FILE

The VPS system stores system errors detected during on line service in the Error Log File inside the hard disk drive. The Error Log File can be displayed on the data terminal by entering the Utility Command "ELOG". System errors detected by VPS during operation are shown in Table 5 - 3. There are two different kinds of errors, warning and fatal error. Warning error can continue to operate automatically by VPS rejecting the generated error fact by itself. In case of fatal error, VPS cannot reject the generated error fact, therefore, the VPS system falls in the condition of Off Line.

Table 5-3. Types of Errors when On Line Service.

Type	Device	Error	Descriptions
Warning	CPU	MEM-GET	This message is dependent on the system software algorithm. Hardware logic has no problem.
	DISK	DATA R/W (XX:YYYY)	There is a data transfer error between the Hard Disk Drive and the Microprocessor. XX means the error code YYYY means the error sector number
	DSPn (*1)	FIFO	Status error on a DSP card. The DSP i/f logic on the DSP card has trouble. It's i/f is between IC101 and IC109.
Fatal	CLOCK		Real Time Clock (IC308) access error.
	DSPn (*1)	SCAN	Status error on a DSP card. The Microprocessor i/f on the DSP card has trouble. It's i/f is between CN101 and IC101.
Warning or Fatal	CPU	APPLICATION (%) (%) means port No.	There is a system error. If this error is detected by the VPS, please inform.

(*1) "n" means DSP chip number in the system

n = 1 : IC109A of the DSP card in SLOT #1, n = 2 : IC109B of the DSP card in SLOT #1

n = 3 : IC109A of the DSP card in SLOT #2, n = 4 : IC109B of the DSP card in SLOT #2

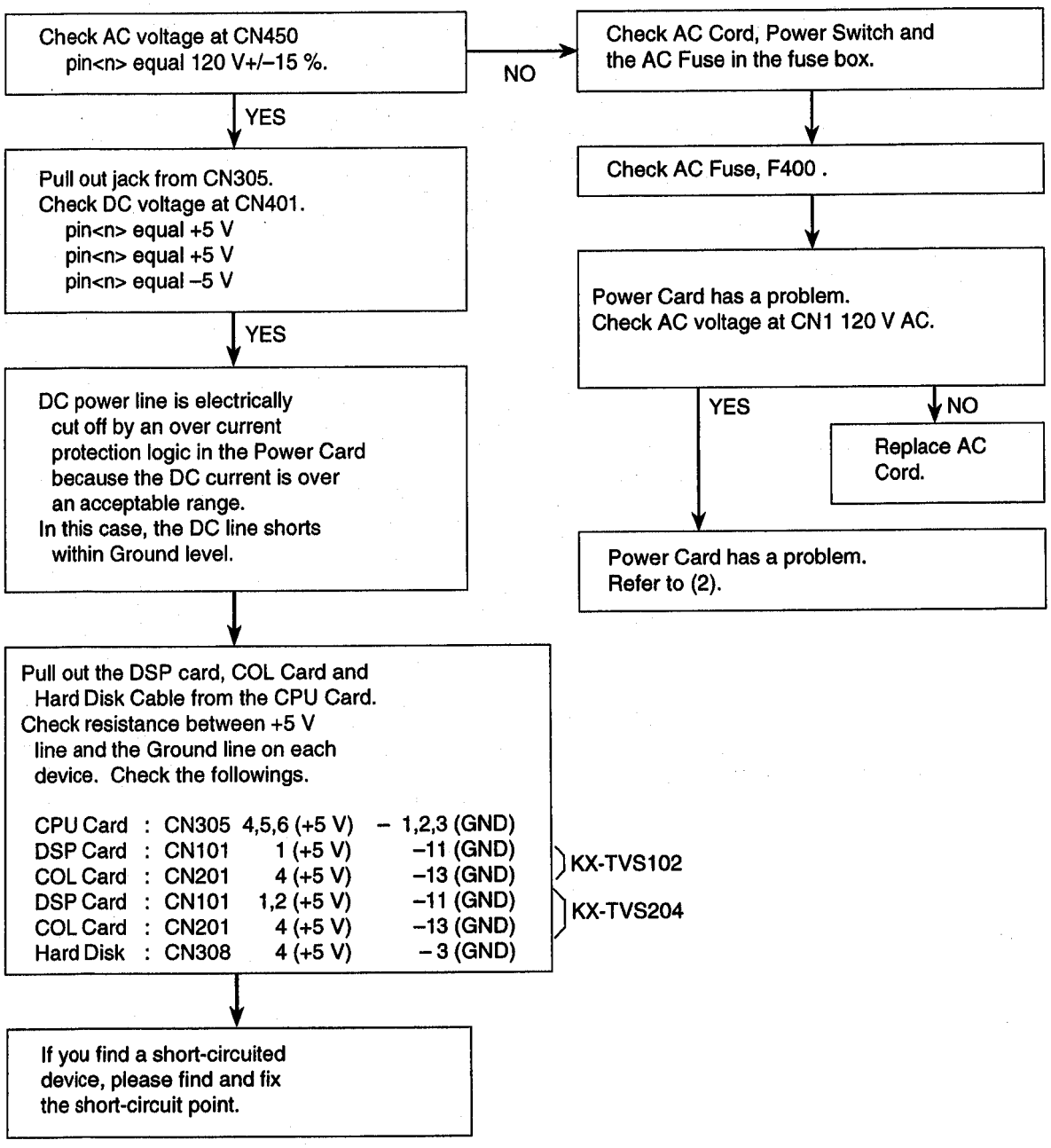
4. TROUBLESHOOTING GUIDE

This section provides the information on troubleshooting.

4-1. No Operation

(1) Power Indicator does not light up in spite of Power ON.

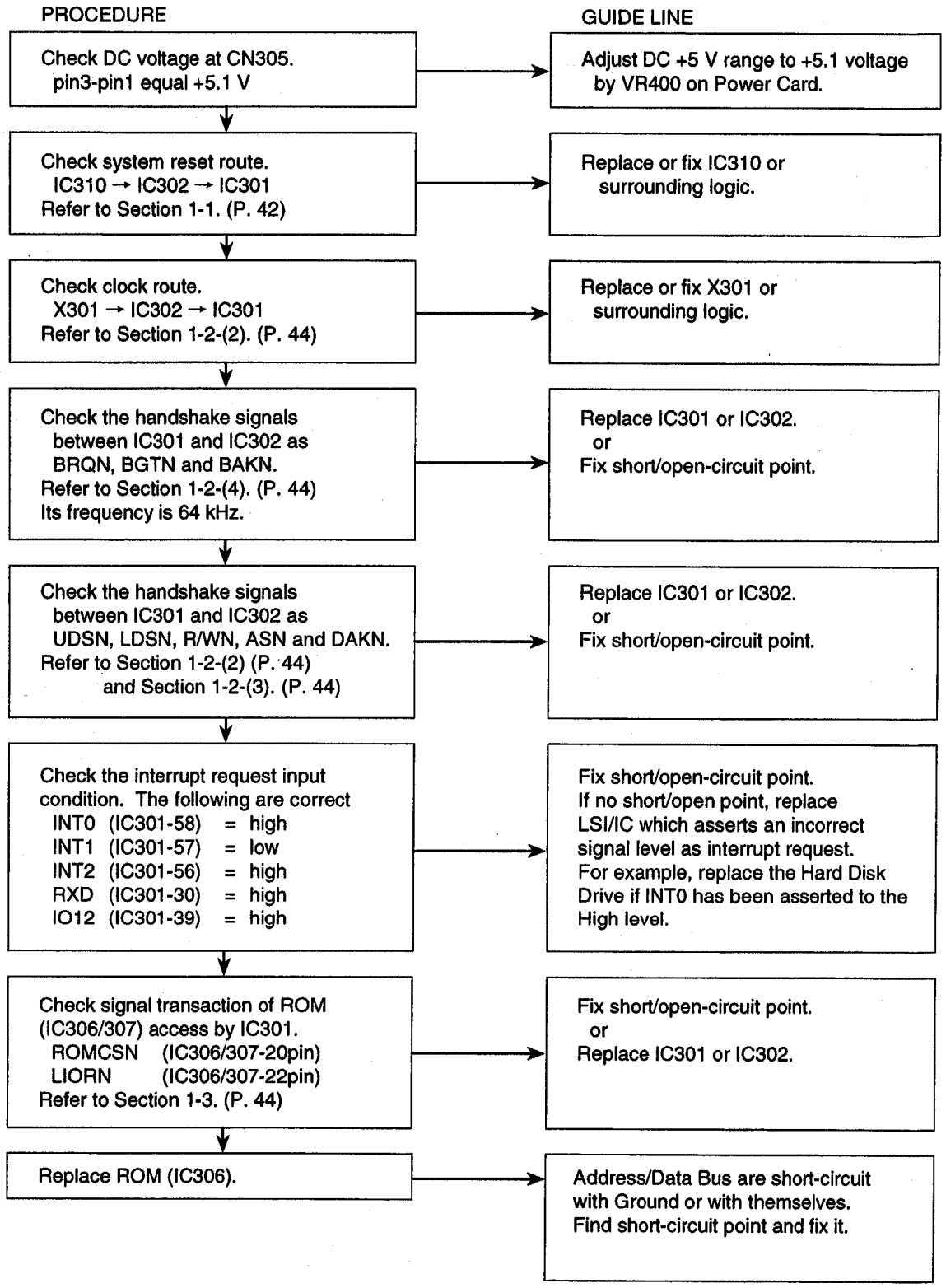
In this case, DC voltage which is supplied to CPU Card is not an acceptable range.
Check supplied DC voltage route to the CPU Card from the AC Inlet as follows.



Check : If the Hard Disk Cable is misattached to the connector on the CPU Card, +5 V line will be shorted to Ground level. Check its connection between the Cable and the CPU Card/Hard Disk Drive.

(2) The Power Indicator does not blink at the power up sequence even though the Power Card has no Problem.

In this case, a micro processor on the CPU card does not runn on a ROM based-program.



(3) The Power Indicator informs the Hardware Error by the blinking sequence at the power up self diagnostic. Please refer to Section 1-(2) (P. 92) and Section 2. (P. 93)

In this case, the CPU Card or Hard Disk Drive has a problem. Please connect the Data Terminal to the VPS, and restart the system. The Data Terminal provides an error status on the screen display.

SCREEN DISPLAY on a Data Terminal and Procedure	GUIDE LINE
RAM R/W ERROR IC304/305/307/309 or an around logic has a problem. Refer to Section 1-4. (P. 49) Check voltage to system memory. IC304/305/307/309pin-1, 14 = +5 V Check the control signal transaction as RASON, CASN, MOEN, LWEN and UWEN. There are driven by IC302. Check memory address bus transaction as MA <9-0>. They are driven by IC302. Replace IC304 or IC305.	Check +5 V pattern Replace IC302 if IC302 does not assert the control signals. or Fix short-circuit point.
ROM ERROR IC306 has a problem. Please refer to Section 1-3. (P. 47) ROM interface logic is no problem because a Microprocessor is running on this ROM (IC306) based program. Replace IC306 and then restart.	If failure occurs in spite of replacing IC306. The higher address bus line is short with +5 V, ground or themselves. Fix short-circuit point.
DISK ERROR: Initialize Error!! Hard Disk Drive or interface logic on the CPU Card has a problem. Refer to Section 1-9. (P. 61) Check the connection between the HDD and CPU. Replace Hard Disk Drive and restart. Check the signal transaction of CN301. RESET, CS <1-0>, IOR, IOW, A <2-0> and D <15-0>.	Re-attach a disk cable. Fix short/open- circuit point or Replace driver ICs as IC312, 313, 314 and 315.

DISK ERROR: No System!! Hard Disk Drive is not installed to a system program.	Install a system program by using an Utility Com'd.
DISK ERROR: Program Load Error!! Microprocessor failed to load a system program from the Hard Disk Drive.	Replace Hard Disk Drive.
DISK ERROR: Program Sum Error!! A loading program has an error pattern. It is a strange media error in the drive.	Replace Hard Disk Drive.
No CO Cards are active!! The expansion bus interface on the CPU Card or DSP Card has a problem. At first, find a error card by replacing the CPU and DSP Card. If the CPU Card has a problem., Check the expansion bus interface Refer to Section 1-10. (P. 67) If the DSP Card has a problem, confirm ELOG file by Data Terminal. If SCAN Error, check the CPU Card interface. Refer to Section 2-2. (P. 81) If FIFO Error, check the DSP interface. Refer to Section 2-3 (P. 81) and 2-4. (P. 81)	Fix short/open-circuit point. Replace driver ICs as IC316, 317 or 318. Replace driver ICs as IC102, 103, 104 or 105. Replace ROM or DSP as IC107, 108 or IC109.

(4) The ELOG file has a message in the Hardware Error at the On Line Service.
Please refer to Section 3. (P. 93)

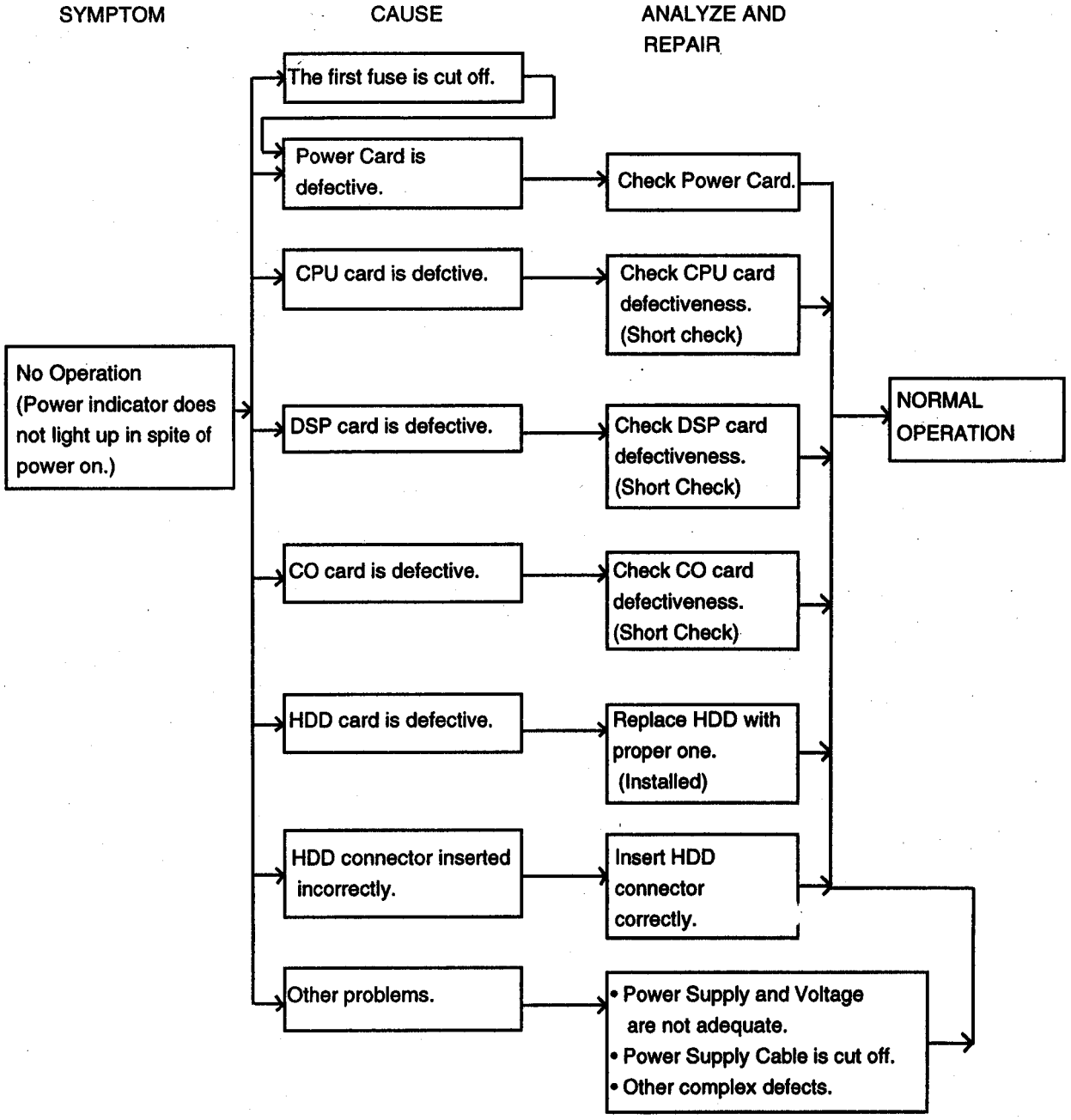
SCREEN DISPLAY on the Data Terminal and Procedure	GUIDE LINE
DISK DATA R/W (XX:YYYY) There is a data transfer error between the Drive and Microprocessor on the CPU Card. Refer to Section 1-9. (P. 61) Check the connection between the HDD and CPU. Replace Hard Disk Drive and then restart. Check the signal transaction of CN301. RESET, CS <1-0>, IOR, IOW, A < 2-0 > and D <15-0>.	Re-attach the disk cable. Fix short/open-circuit point or Replace driver ICs as IC312, 313, 314 and 315

DSPn FIFO Status error in the DSP Card. The DSP interface logic has a problem. It is between CN101 and IC101. Refer to Section 2-3 (P. 81) and 2-4. (P.81)	Replace ROM or DSP as IC107, 108 or IC109.
DSPn SCAN Status error in the DSP Card. The CPU Card interface has a problem. It is between CN101 and IC101. Refer to Section 2-2. (P. 81)	Replace driver ICs as IC102, 103, 104 or 105.
CLOCK The Real Time Clock IC (IC308) has an access error. Refer to Section 1-7. (P. 56)	Replace IC308.

(5) The VPS can not receive/transmit messages from/to PBX.

In this case, the data transfer route of the voice message has a problem. Its route is the serial voice port between the CPU Card and DSP Card. Refer to Section 1-10-(5). (P. 67)

PROCEDURE		GUIDE LINE
Check 4 MHz clock at IC101-pin40.	NO	Check 4 MHz route from IC301-pin85.
Check signal transactions of CN302 UVCN (48), UVAN (47), UVDN (46), DVCN (42), DVDN (43) and SYNCN (41).	NO	Check signal route from IC302 to IC101.
Check signal transactions of the CODEC interface.		Check signal route from IC109 to IC241.
Check signal transactions of the analog interface. Refer to Section 3. (P. 85)		Check analog signal route from IC109 to T-R.



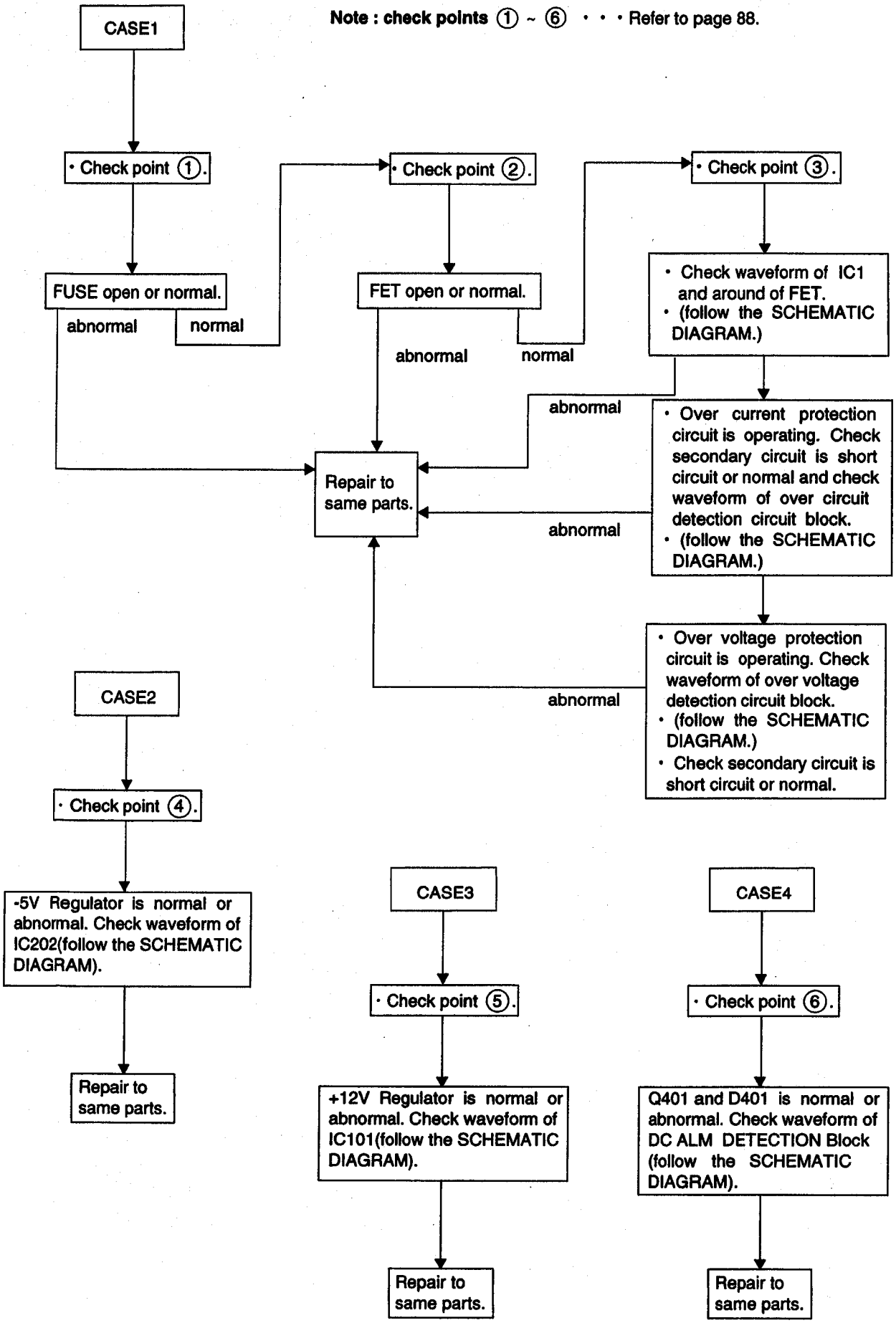
4 - 2. Power Supply

· Pull out DC supply cable and check DC voltage at CN101 Connector.

CN101

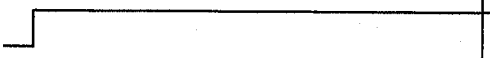
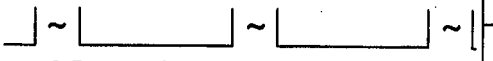
Pin Number	Voltage
1	GND
2	GND
3	GND
4	5.13V(4.85V~5.25V)
5	5.13V(4.85V~5.25V)
6	5.13V(4.85V~5.25V)
7	5.3V(5.0V~5.5V)
8	5.3V(5.0V~5.5V)
9	GND
10	-5V
11	GND
12	12V

CASE1: ALL DC voltage is not outputted.
CASE2: -5V DC voltage is not outputted.
CASE3: 12V DC voltage is not outputted.
CASE4: Pin number 7 (ALM) DC voltage is not outputted.


CASE1
Note : check points ① ~ ⑥ • • • Refer to page 88.
• Check point ①.
• Check point ②.
• Check point ③.
FUSE open or normal.
abnormal
normal
FET open or normal.
abnormal
normal
• Check waveform of IC1 and around of FET.
• (follow the SCHEMATIC DIAGRAM.)
abnormal
Repair to same parts.
• Over current protection circuit is operating. Check secondary circuit is short circuit or normal and check waveform of over circuit detection circuit block.
• (follow the SCHEMATIC DIAGRAM.)
abnormal
• Over voltage protection circuit is operating. Check waveform of over voltage detection circuit block.
• (follow the SCHEMATIC DIAGRAM.)
• Check secondary circuit is short circuit or normal.
abnormal
CASE2
• Check point ④.
-5V Regulator is normal or abnormal. Check waveform of IC202(follow the SCHEMATIC DIAGRAM).
Repair to same parts.
CASE3
• Check point ⑤.
+12V Regulator is normal or abnormal. Check waveform of IC101(follow the SCHEMATIC DIAGRAM).
Repair to same parts.
CASE4
• Check point ⑥.
Q401 and D401 is normal or abnormal. Check waveform of DC ALM DETECTION Block (follow the SCHEMATIC DIAGRAM).
Repair to same parts.

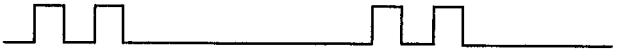
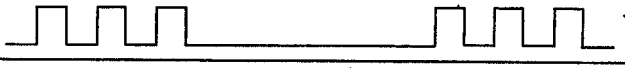
Power LED's ON and OFF is abnormal

<POWER LED ON and OFF pattern>
[Normal LED ON and OFF pattern]

Phase	Screen Display	LED Condition
Power ON		ON 
System Data is under construction	System Set up	ON and OFF  0.25 second 0.25 second
After start up		
May apply	** ON LINE MODE **	ON  → Normal
May not apply (1)	** OFF LINE MODE **	ON and OFF  → ③ 0.5 second 0.5 second
May not apply (2)	** OFF LINE MODE **	ON and OFF  → ④ 0.5 second 3.5 second

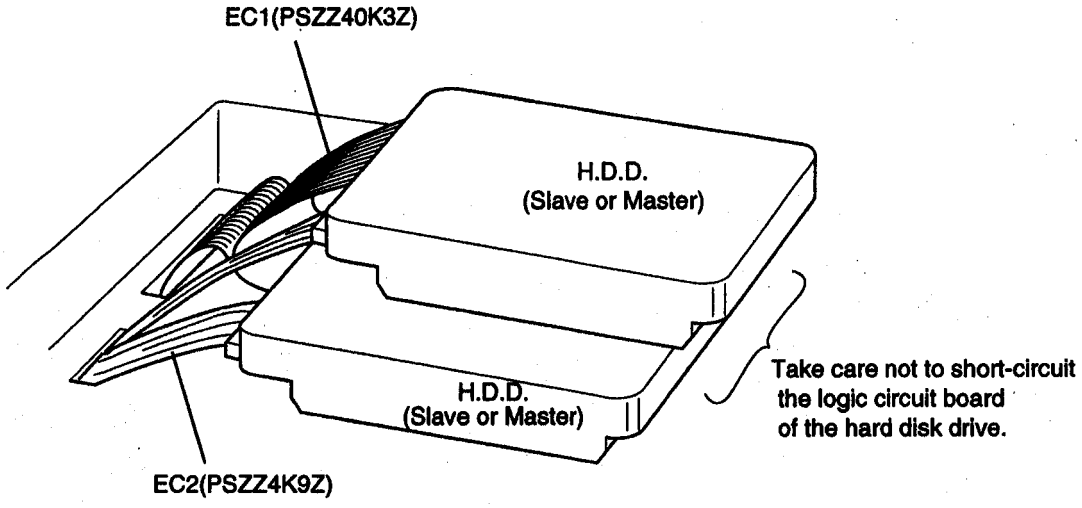
Remarks May not apply (1) is the condition of PITS communication circuit being out, can recover condition.
May not apply (2) is No CO/DSP card or error generation in starting up, etc. with serious error and cannot recover.

[LED ON and OFF pattern at generated error]
In case an error generates from the time Power Source is ON in to system data in under construction, the LED displays as follows.

Error	Screen Display	LED Condition
DC Alarm		ON and OFF  → ⑤
RAM error		ON and OFF  → ⑥
ROM error	ROM ERROR : Sum Error!!	ON and OFF  → ⑦
HDD error (Initialize)	DISK ERROR : Initialize Error!!	ON and OFF  → ⑧
HDD error (No-system)	DISK ERROR : No System!!	ON and OFF  → ⑨
HDD error (Read in error)	DISK ERROR : Program Load Error!!	ON and OFF  → ⑩
HDD error (Check sum)	DISK ERROR : Program Sum Error!!	ON and OFF  → ⑪

H.D.D. INSTALLATION PROCEDURE

1. HOW TO USE THE H.D.D. COPY CABLE



Set and connect the unit serving as the copy source to function as the master and the unit serving as the copy destination to function as the slave and, after startup using the master disk, input the copy commands shown below from the terminal and copy the data.

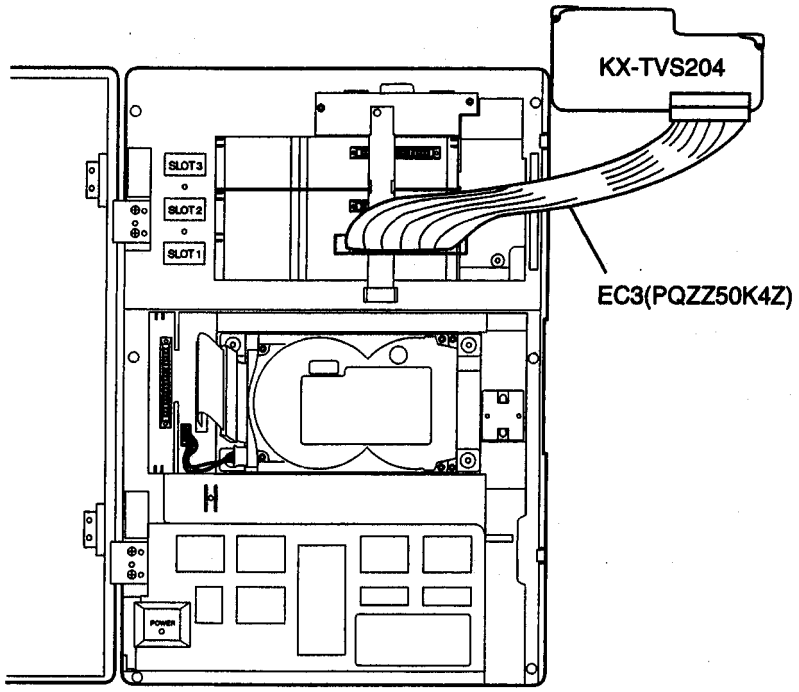
1. To start up with POWER ON Master HDD.
2. Select "1. ASCII TERMINAL" as Terminal Type.
3. Select "3. Utility Command".
4. Input "KME" and password. (PANASONIC)
5. Input command "SYSD". (Refer to page 105)
6. Data copy is complete after 25 minutes.
7. Put HDD, HDD cable back, then start up with power on.
8. Select the destination with command "PDCT".
9. Installation is complete with Power off --- Power on. Can be used.

For details on the master and slave jumper settings, refer to page 65 or to the Specifications Manual issued by the hard disk drive manufacturer.

2. HOW TO USE THE EXTENSION SLOT CABLE

How to use the expansion slot service cables

Connect the cables to the expansion slot, pull out TVS204, and check the signal waveforms and voltage value.



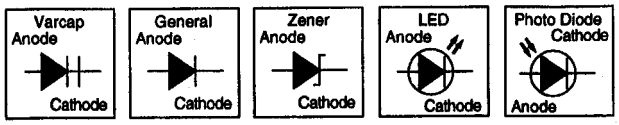
NOTES FOR SCHEMATIC DIAGRAM

1. DC voltage measurements are taken with an electronic voltmeter and oscilloscope from a ground line.

   (Power Switch ON condition
   Voltage Value : V)

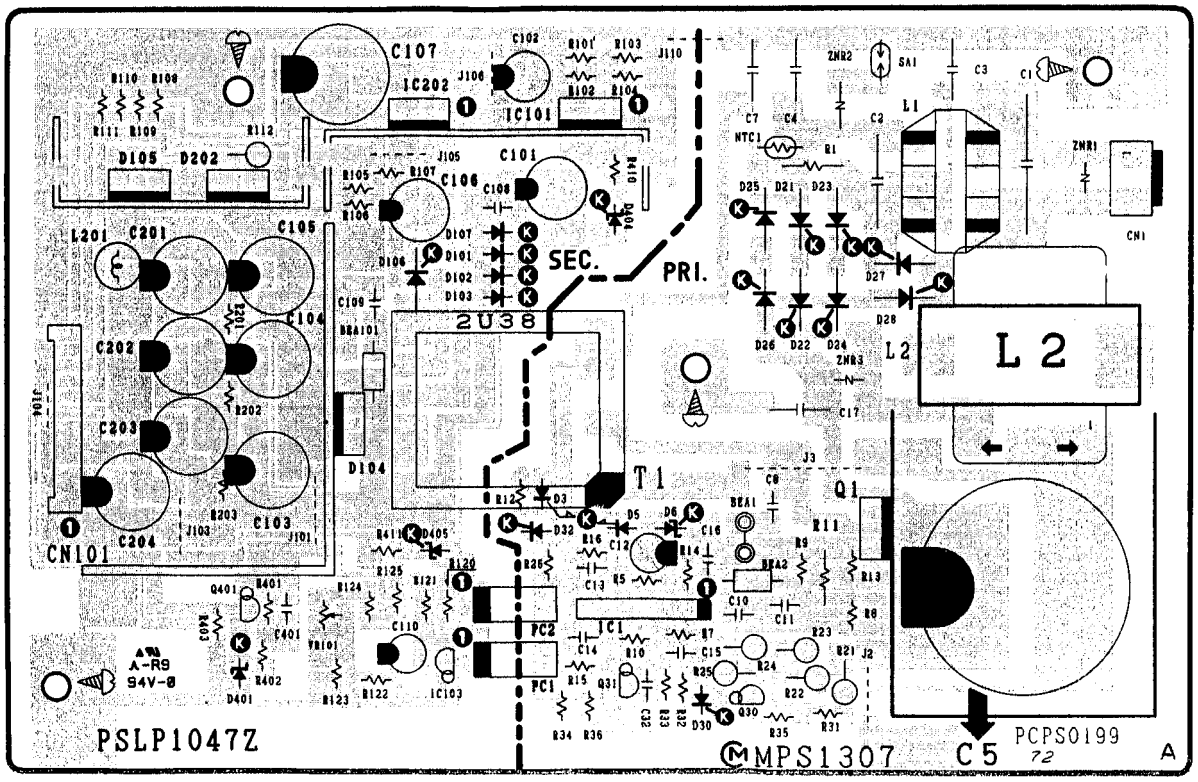
2. This schematic diagram may be modified at any time with the development of new technology.

3. Important safety notice
   The shaded area on this schematic diagram incorporates special features important for protection from fire and electrical shock hazards. When servicing it is essential that only manufacturer's specified parts be used for the critical components in the shaded areas of the schematic.

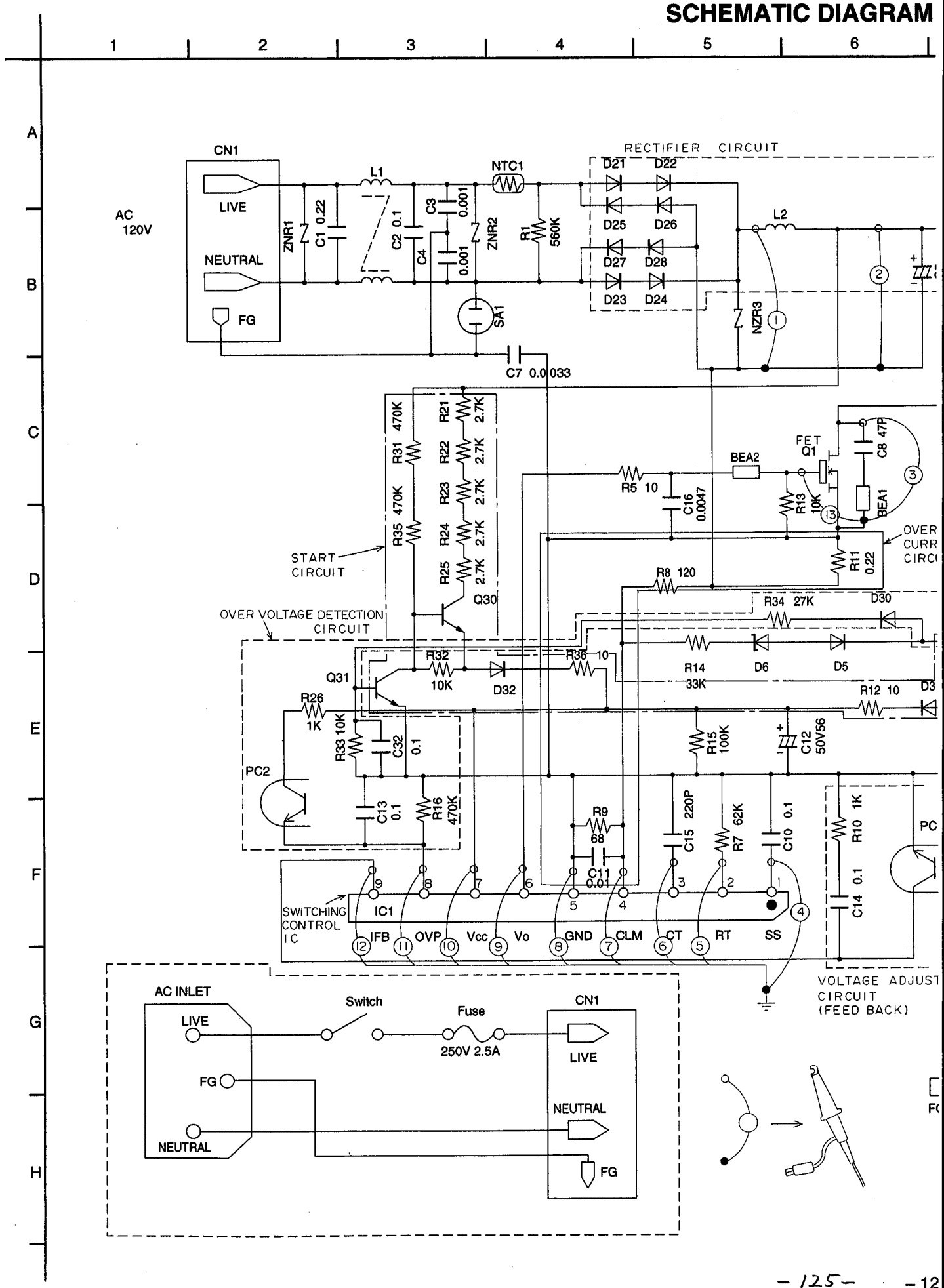
4. 

PRINTED CIRCUIT BOARD (POWER SUPPLY)

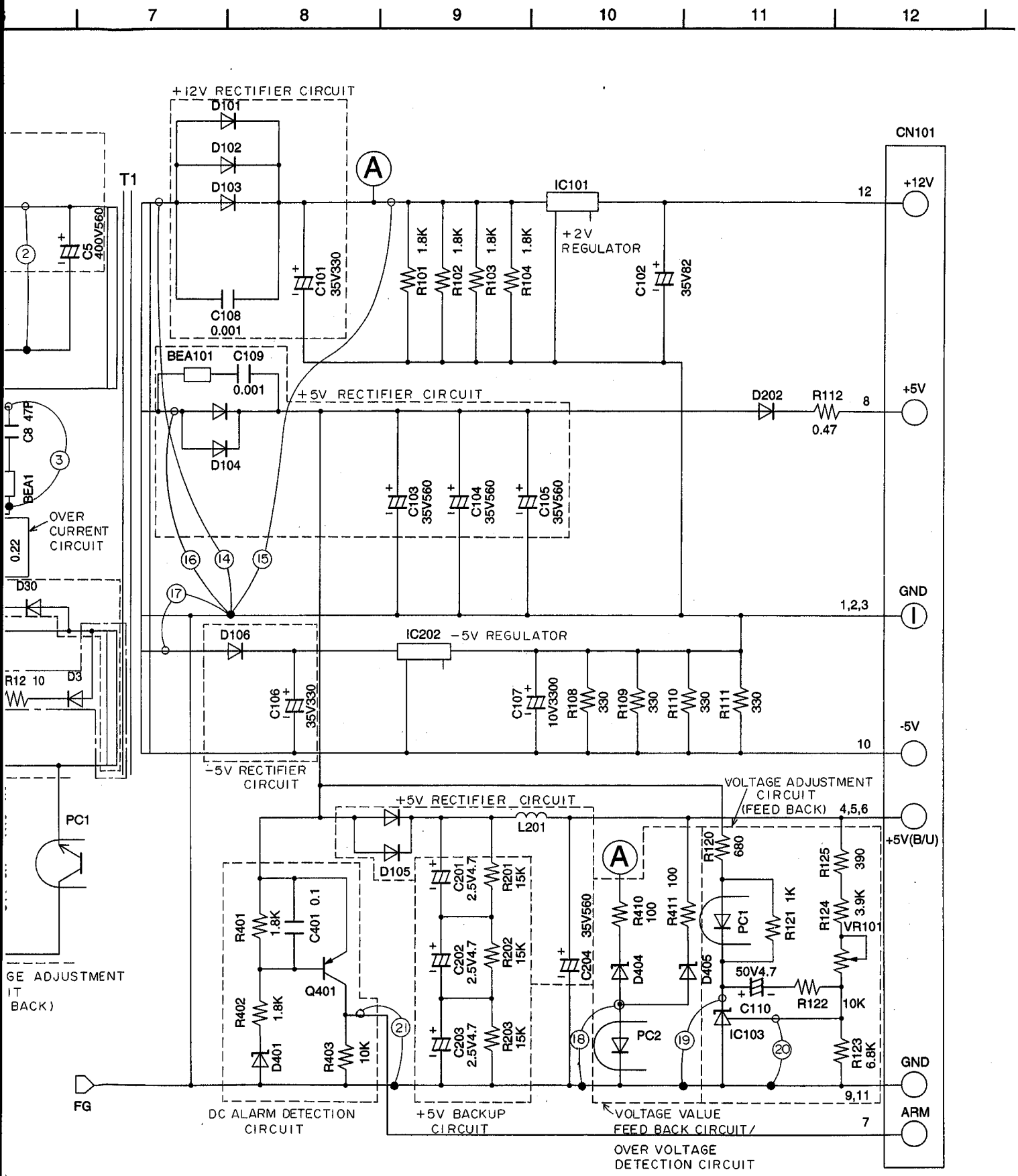
(COMPONENT VIEW)



SCHEMATIC DIAGRAM

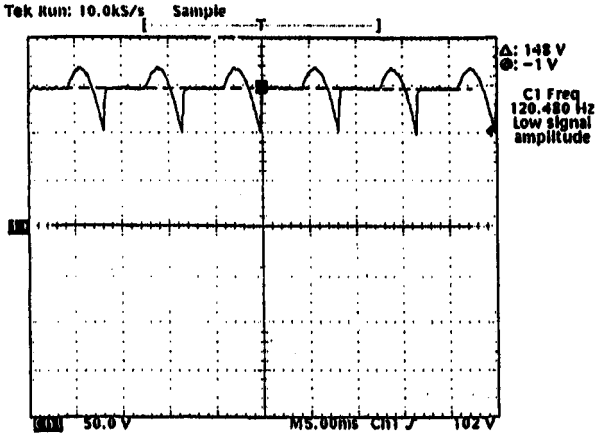


GRAM (POWER SUPPLY)

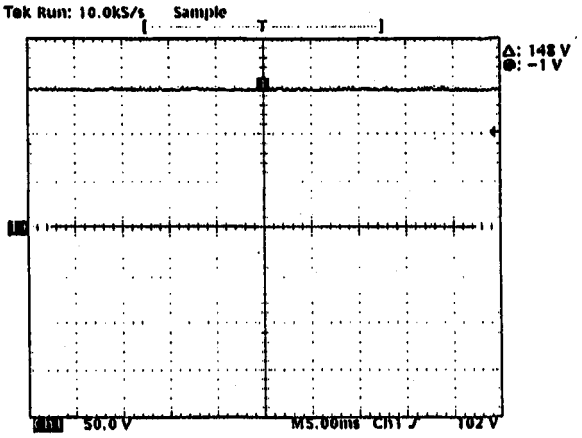


(Waveform of Power card)

① After diode bridge

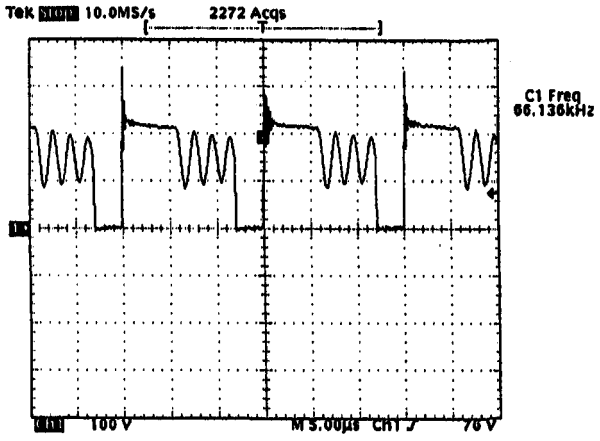


② After rectification

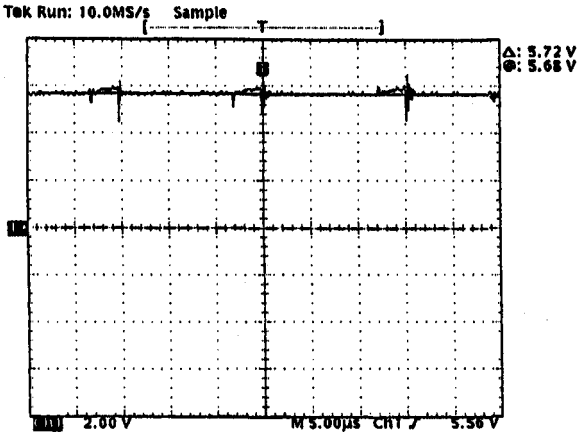


⑦ IC1-C

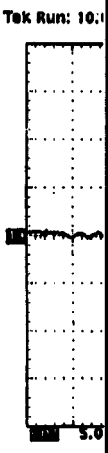
③ FET (D-S)



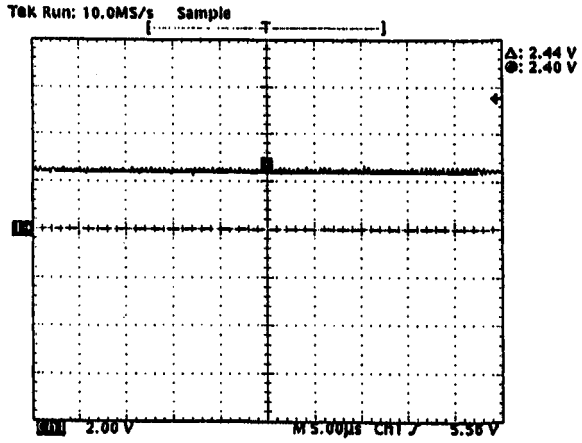
④ IC1-SS



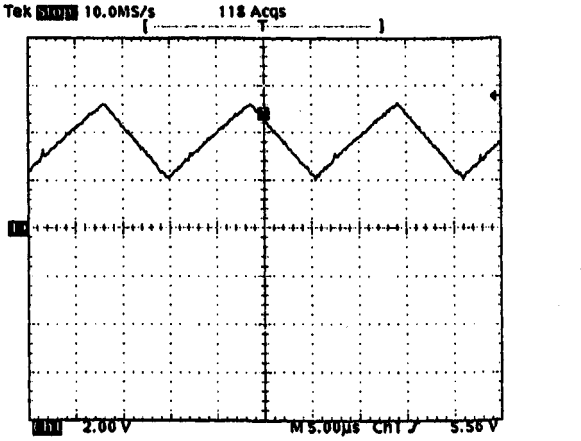
⑨ IC1-V



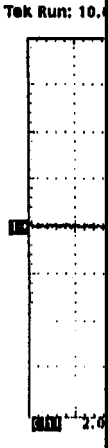
⑤ IC1-RT



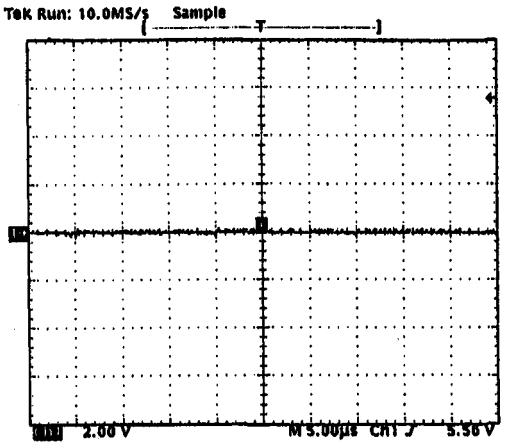
⑥ IC1-CT



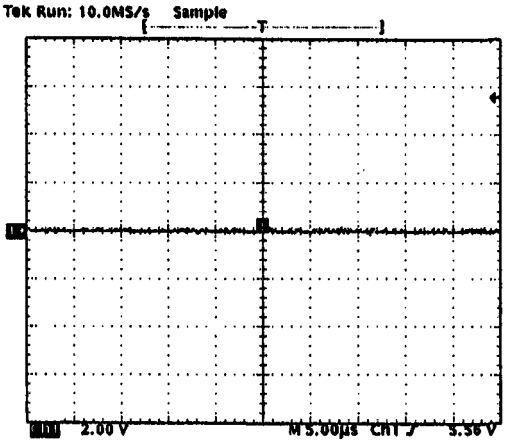
⑪ IC1-O



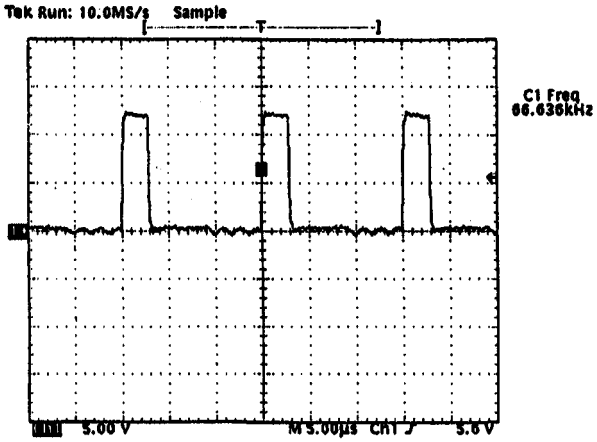
⑦ IC1-CLM



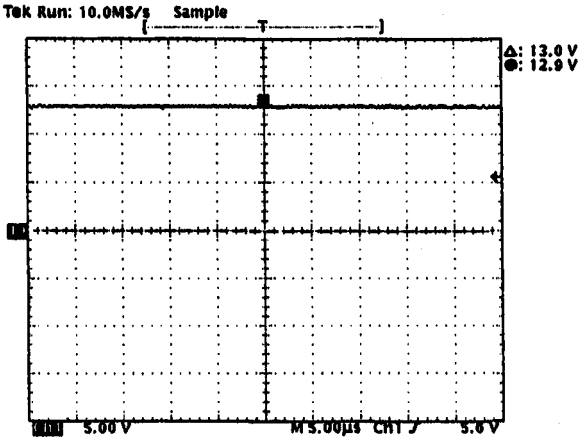
⑧ IC1-GND



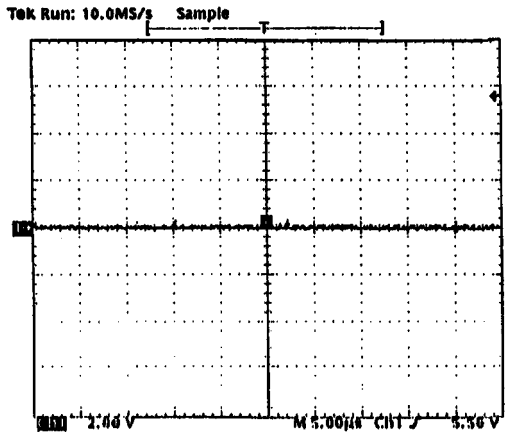
⑨ IC1-Vo



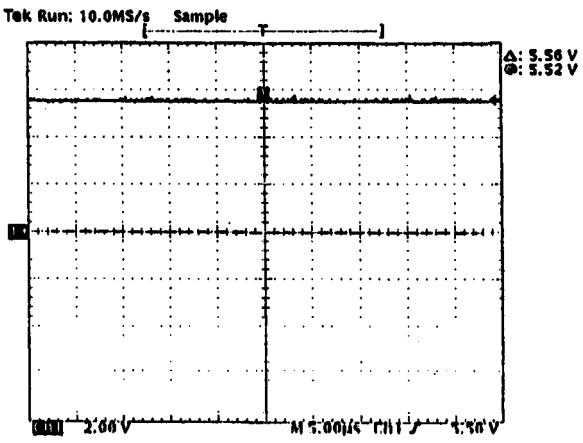
⑩ IC1-Vcc



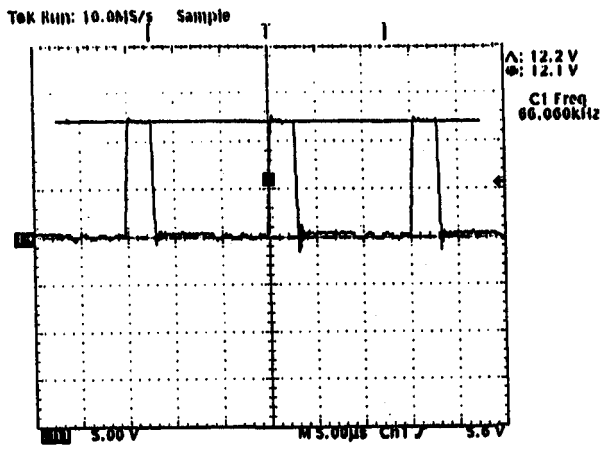
⑪ IC1-OVP



⑫ IC1-IFB



⑬ FET-Gate



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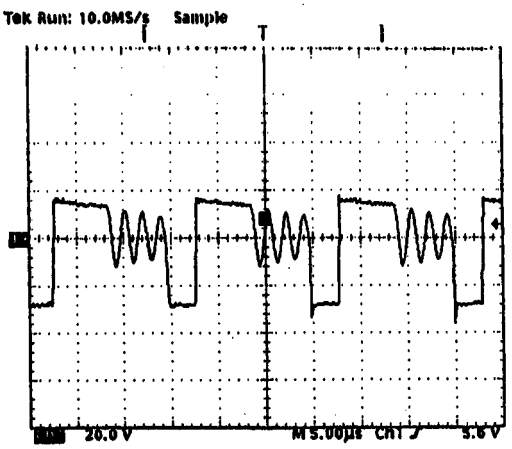

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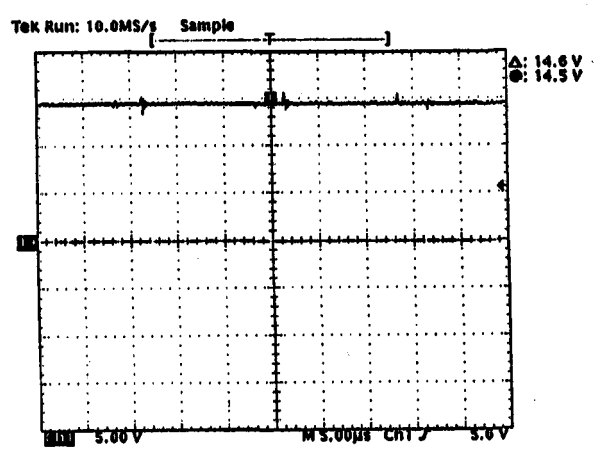
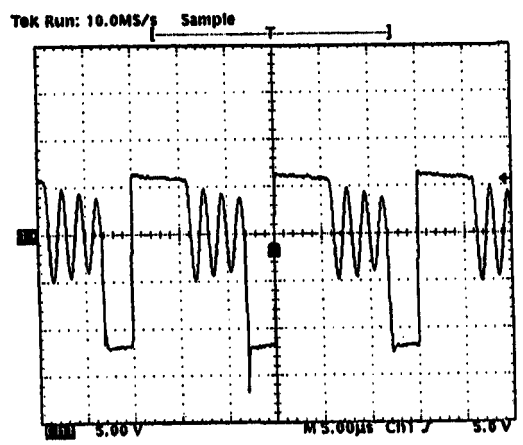
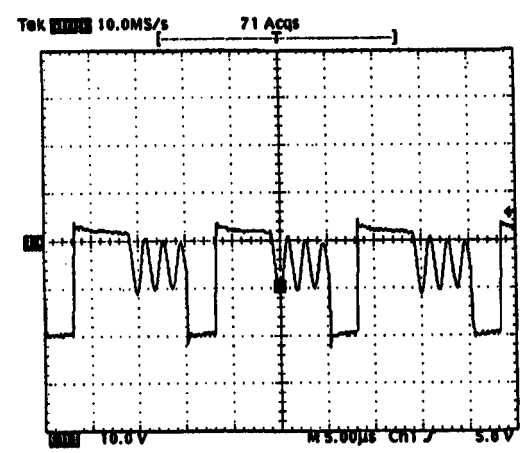


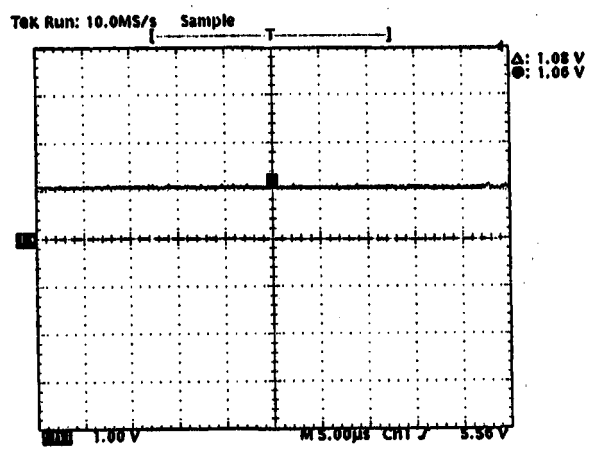
⑯



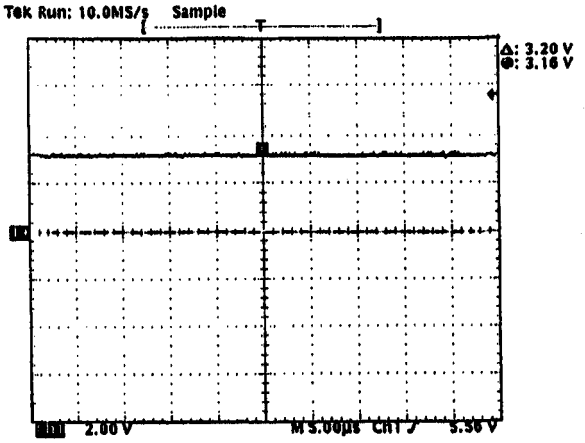
⑰



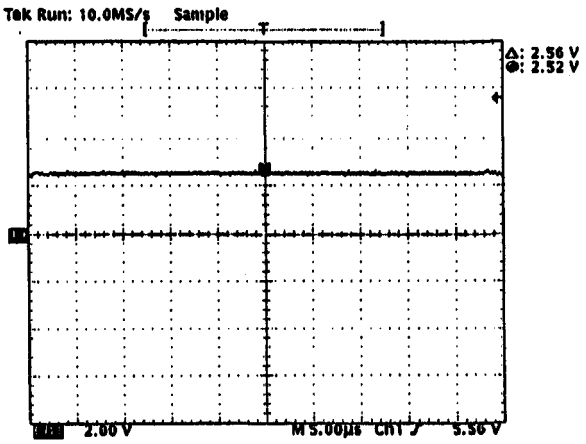
⑱



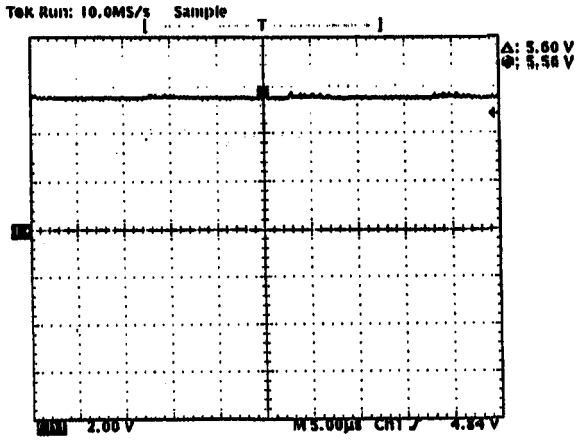
⑲

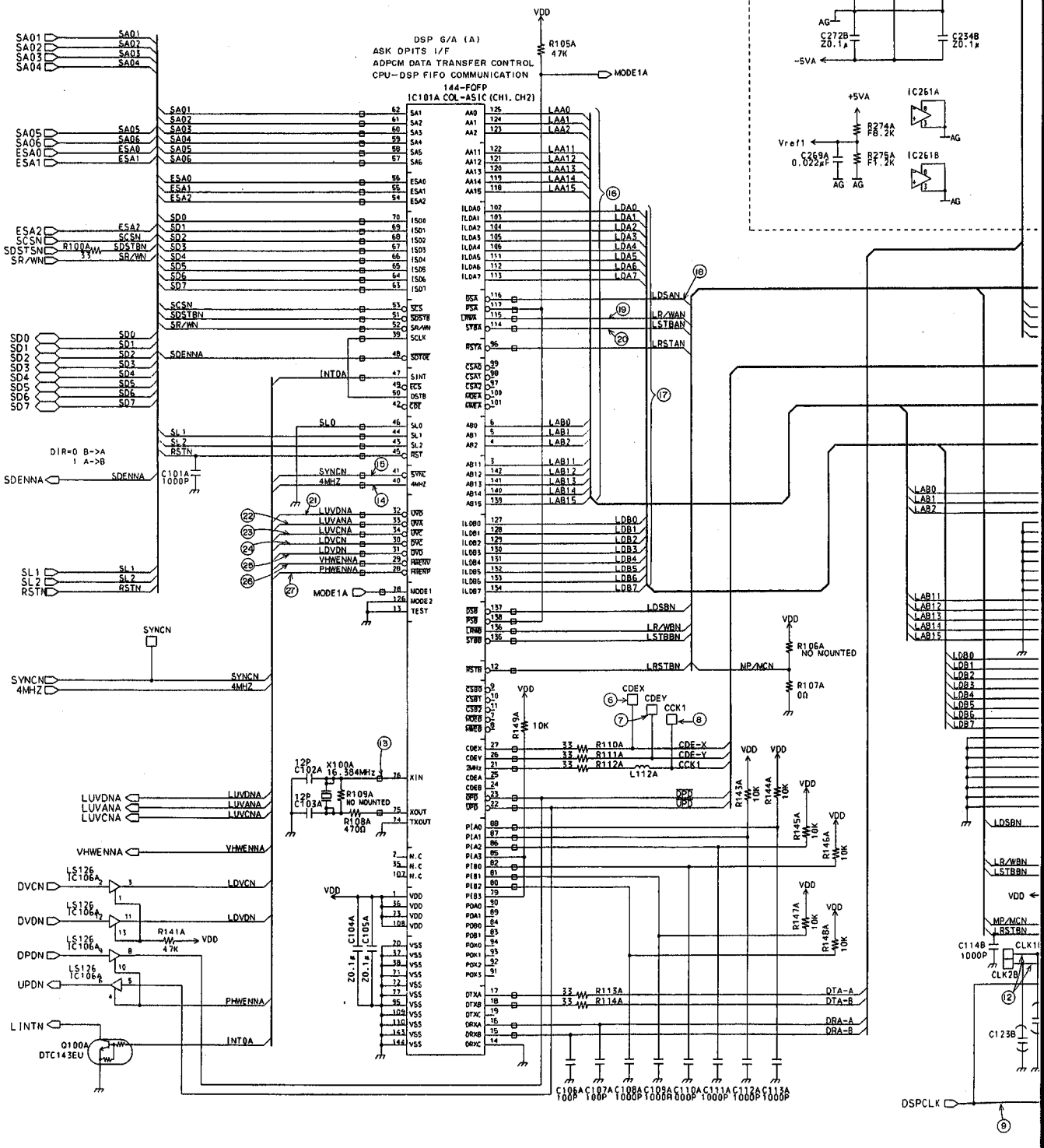

Tek Run: 10.0MS/s Sample
Δ: 3.20 V
@: 3.16 V
2.00 V
M 5.00µs Ch1 ƒ 5.56 V

⑳

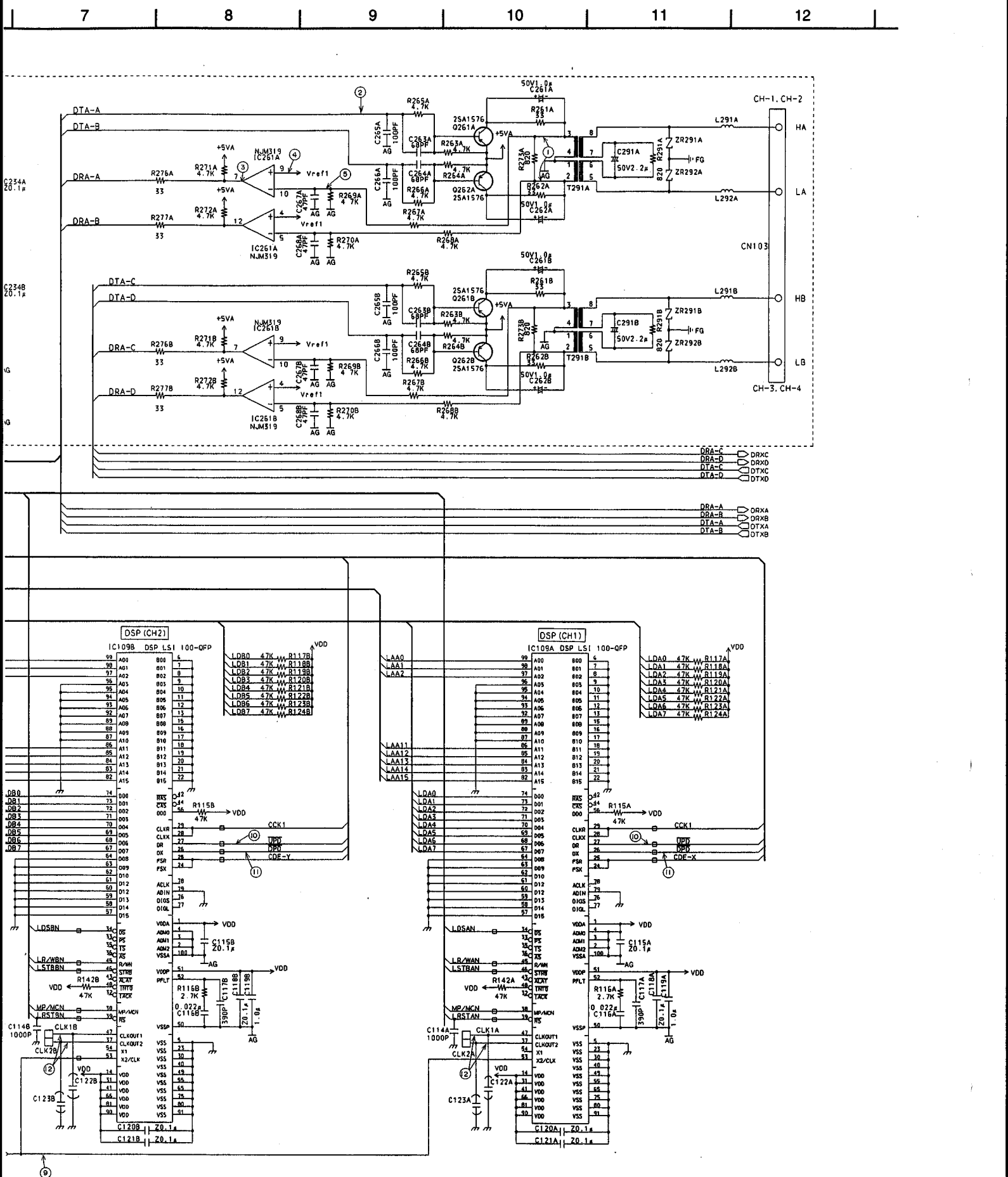

Tek Run: 10.0MS/s Sample
Δ: 2.56 V
@: 2.52 V
2.00 V
M 5.00µs Ch1 ƒ 5.56 V

㉑


Tek Run: 10.0MS/s Sample
Δ: 5.60 V
@: 5.56 V
2.00 V
M 5.00µs Ch1 ƒ 4.84 V


DPITS I/F BLOCK
NJM319 IC261A
NJM319 IC261B
+5VA
-5VA
AG
Vref1
C230A 0.1μ
C233A 0.1μ
C234A 0.1μ
C272A 0.1μ
C230B 0.1μ
C233B 0.1μ
C234B 0.1μ
C272B 0.1μ
C269A 0.022μF
R274A 8.2K
R275A 1.2K
DSP G/A (A)
ASK DPITS I/F
ADPCM DATA TRANSFER CONTROL
CPU-DSP FIFO COMMUNICATION
144-FQFP
IC101A COL-ASIC (CH1, CH2)
R105A 47K
MODE1A
INT0A
SDENNA
SYNCN
4MHZ
LUVDNA
LUVANA
LUVCNA
LDVCN
LDVDN
VHWENNA
PHWENNA
SL1
SL2
RSTN
SCSN
SDSTBN
SR/WN
SDSTSN
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
ESA0
ESA1
ESA2
SA01
SA02
SA03
SA04
SA05
SA06
LAA0
LAA1
LAA2
LAA11
LAA12
LAA13
LAA14
LAA15
LDA0
LDA1
LDA2
LDA3
LDA4
LDA5
LDA6
LDA7
LDSAN
LR/WAN
LSTBAN
LRSTAN
LAB0
LAB1
LAB2
LAB11
LAB12
LAB13
LAB14
LAB15
LDB0
LDB1
LDB2
LDB3
LDB4
LDB5
LDB6
LDB7
LDSBN
LR/WBN
LSTBBN
LRSTBN
MP/MCN
R106A NO MOUNTED
R107A 0Ω
CDEX
CDEY
CCK1
CDE-X
CDE-Y
R110A
R111A
R112A
L112A
R109A NO MOUNTED
R108A 470Ω
X100A 16.384MHz
C102A 12P
C103A 12P
C104A 0.1μ
C105A 0.1μ
R141A 47K
R143A 10K
R144A 10K
R145A 10K
R146A 10K
R147A 10K
R148A 10K
R149A 10K
R113A
R114A
DTA-A
DTA-B
DRA-A
DRA-B
C106A 100P
C107A 100P
C108A 1000P
C109A 1000P
C110A 1000P
C111A 1000P
C112A 1000P
C113A 1000P
C114B 1000P
C123B
CLK1
CLK2B
DSPCLK
LS126 IC106A
LS126 IC106B
DVCN
DVDN
DPDN
UPDN
LINTN
Q100A DTC143EU
DIR=0 B->A
1 A->B
C101A 1000P
R100A 33

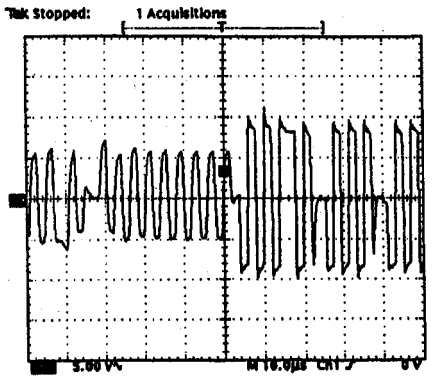
AGRAM (KX-TVS204)



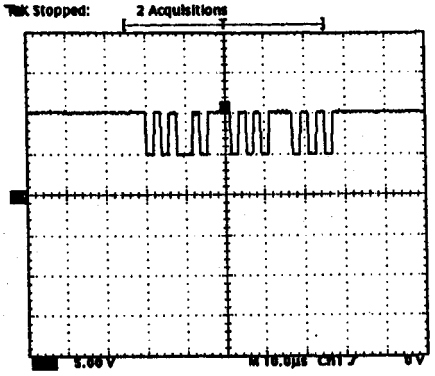
-128-

(Waveform of KX-TVS204)

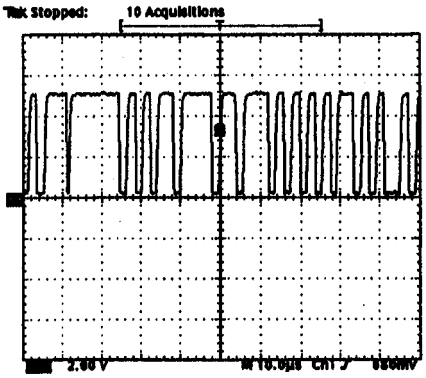
①



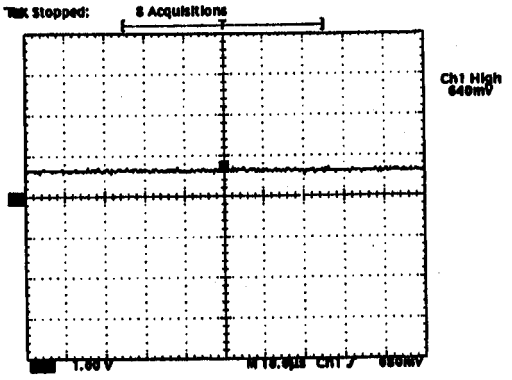
② DTA



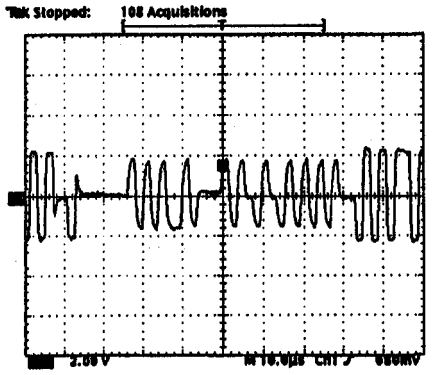
③ DRA



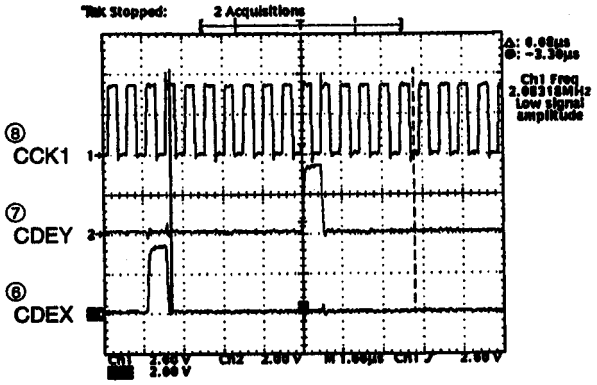
④ Vref



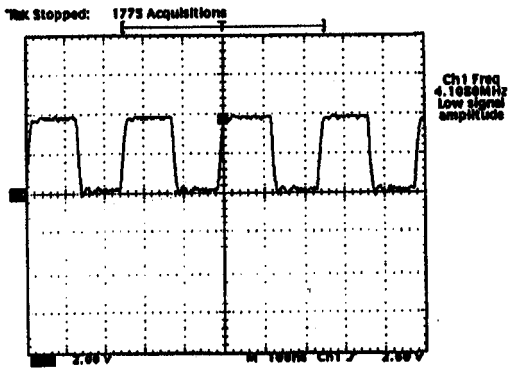
⑤ IC261 input



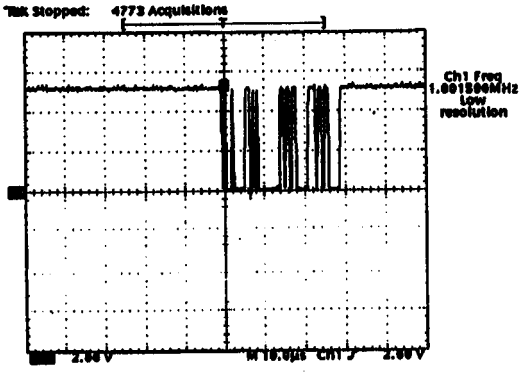
⑥ CDEX, ⑦ CDEY, ⑧ CCK1



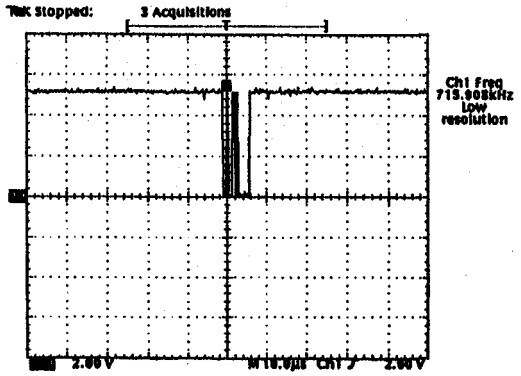
⑨ DSPCLK



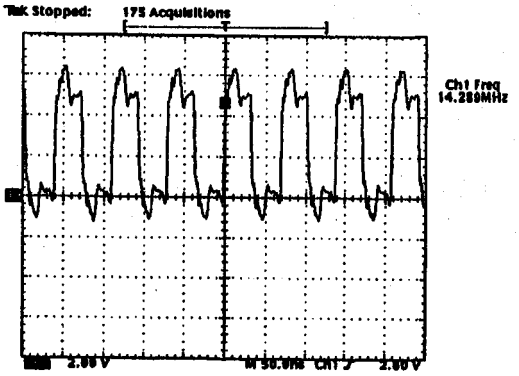
⑩ $\overline{\text{UPD}}$



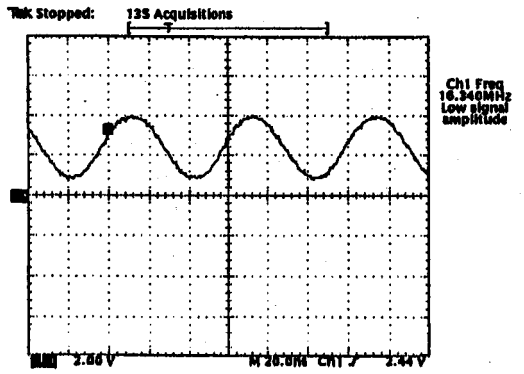
⑪ CDE-Y



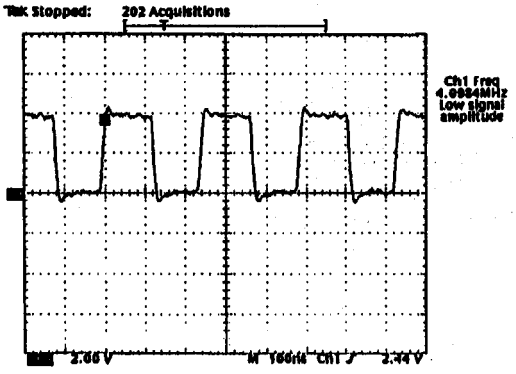
⑫ CLK1, CLK2



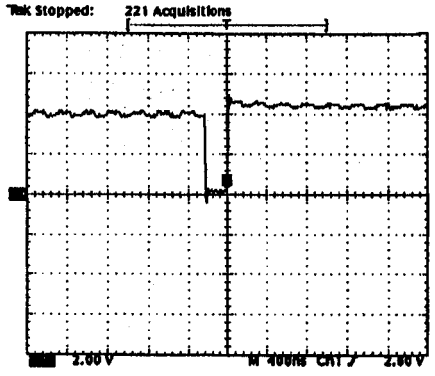
⑬ XIN



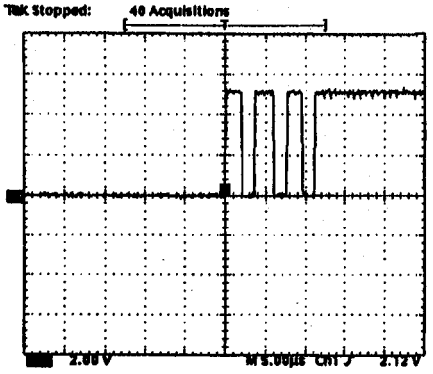
⑭ 4MHz



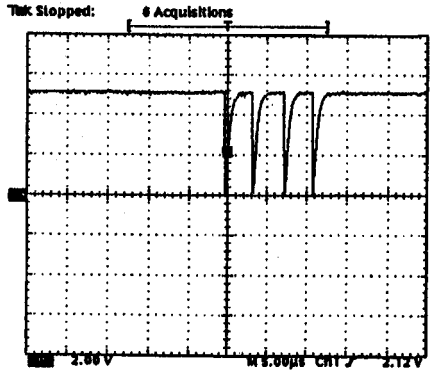
⑮ SYNCN



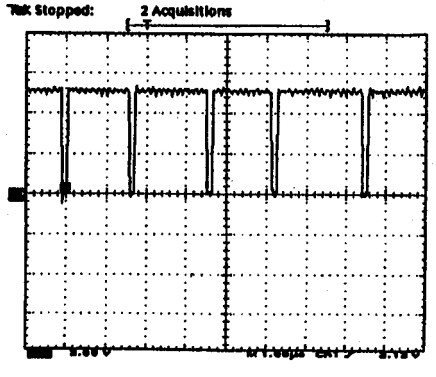
⑯ LAA0~LAA15, LAB0~LAB15



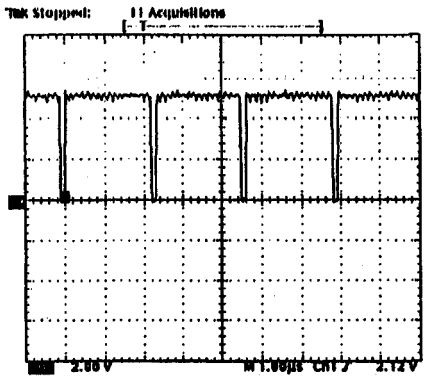
⑰ LDA0~LDA7, LDB0~LDB7



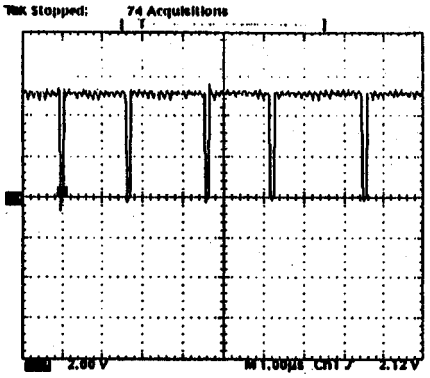
⑱ LDSAN



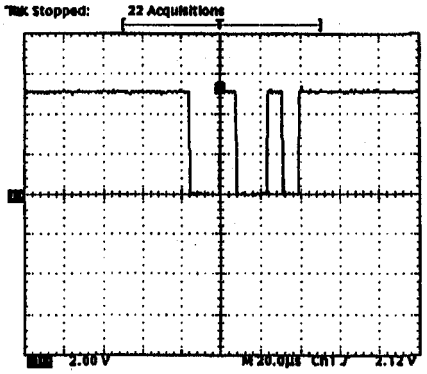
⑲ LR/WAN



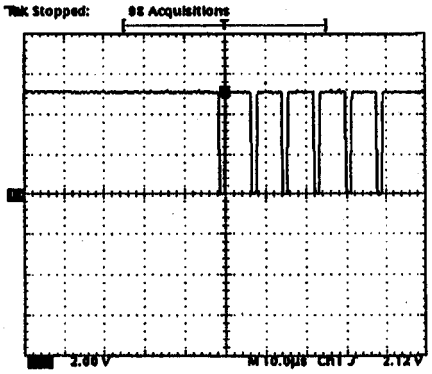
⑳ LSTBAN



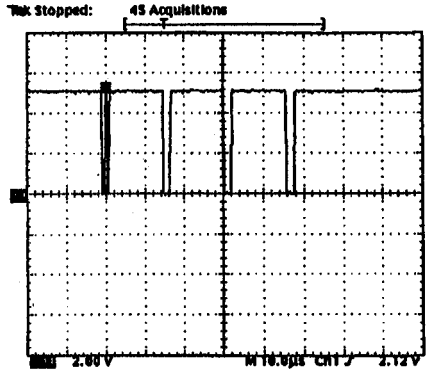
㉑ LUVDNA



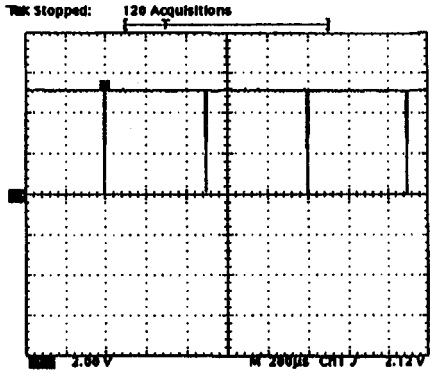
㉒ LUVANA



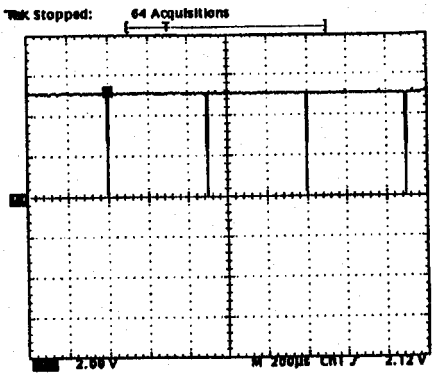
㉓ LUVCNA



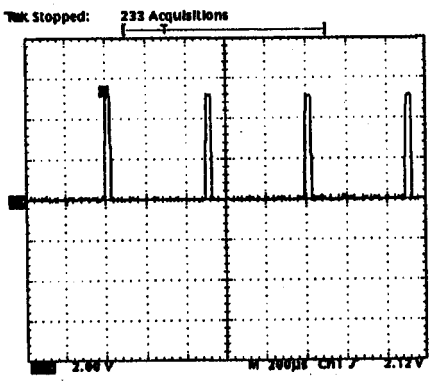
㉔ LDVCN



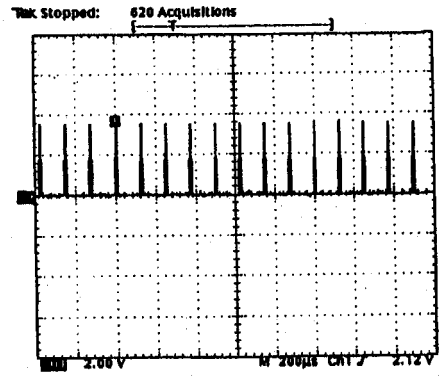
㉕ LDVDN

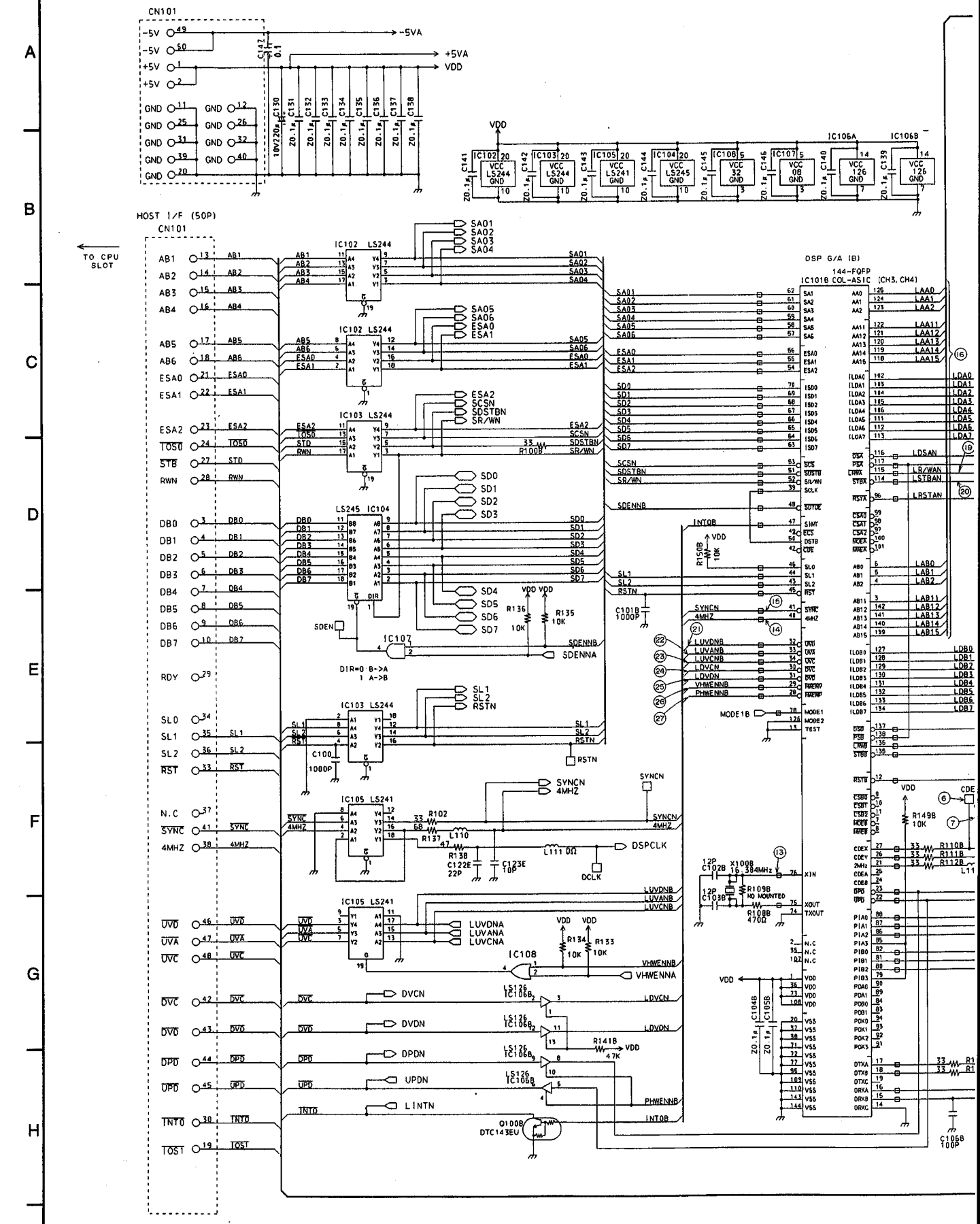


㉖ VHWENNA

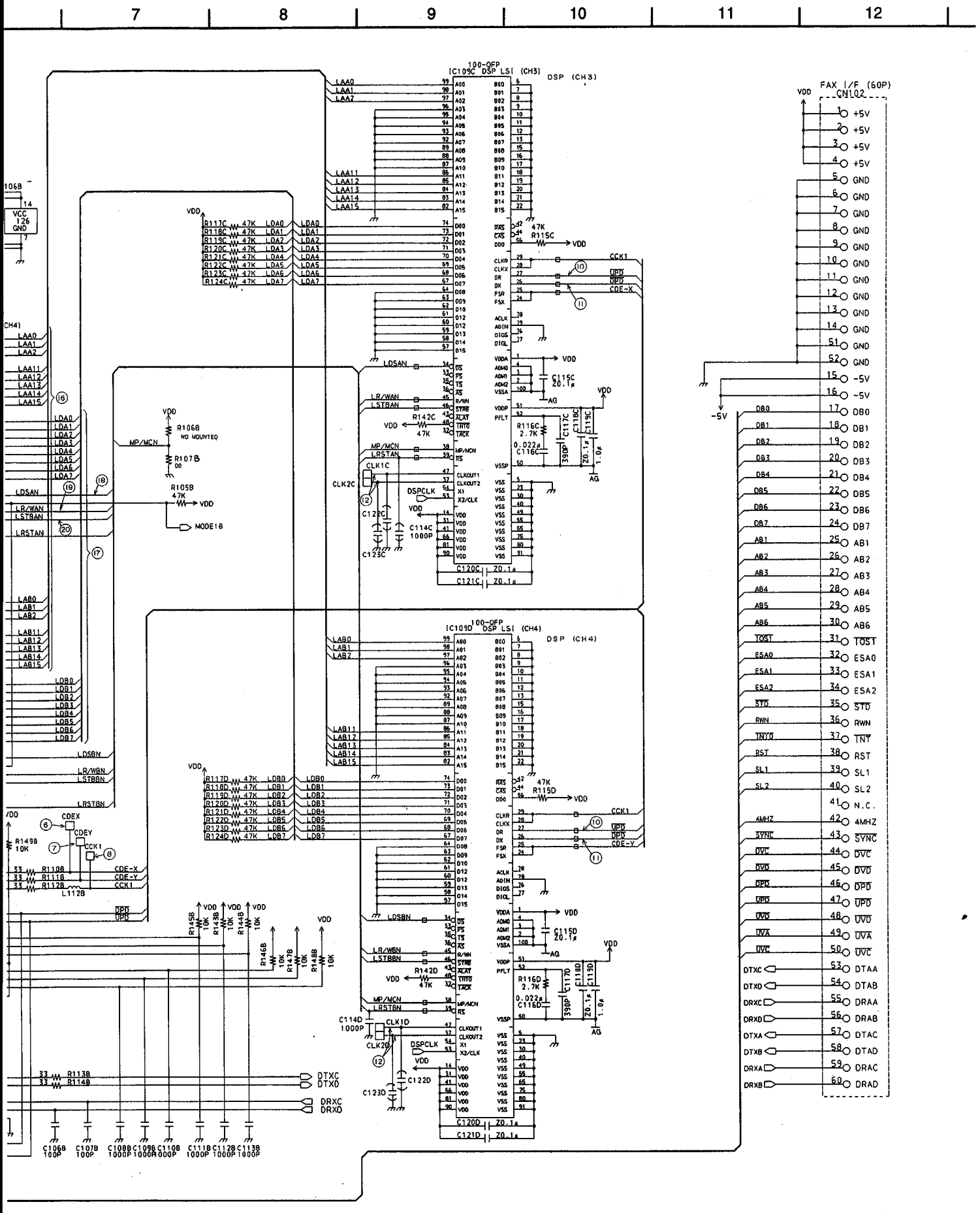


㉗ PHWENNA

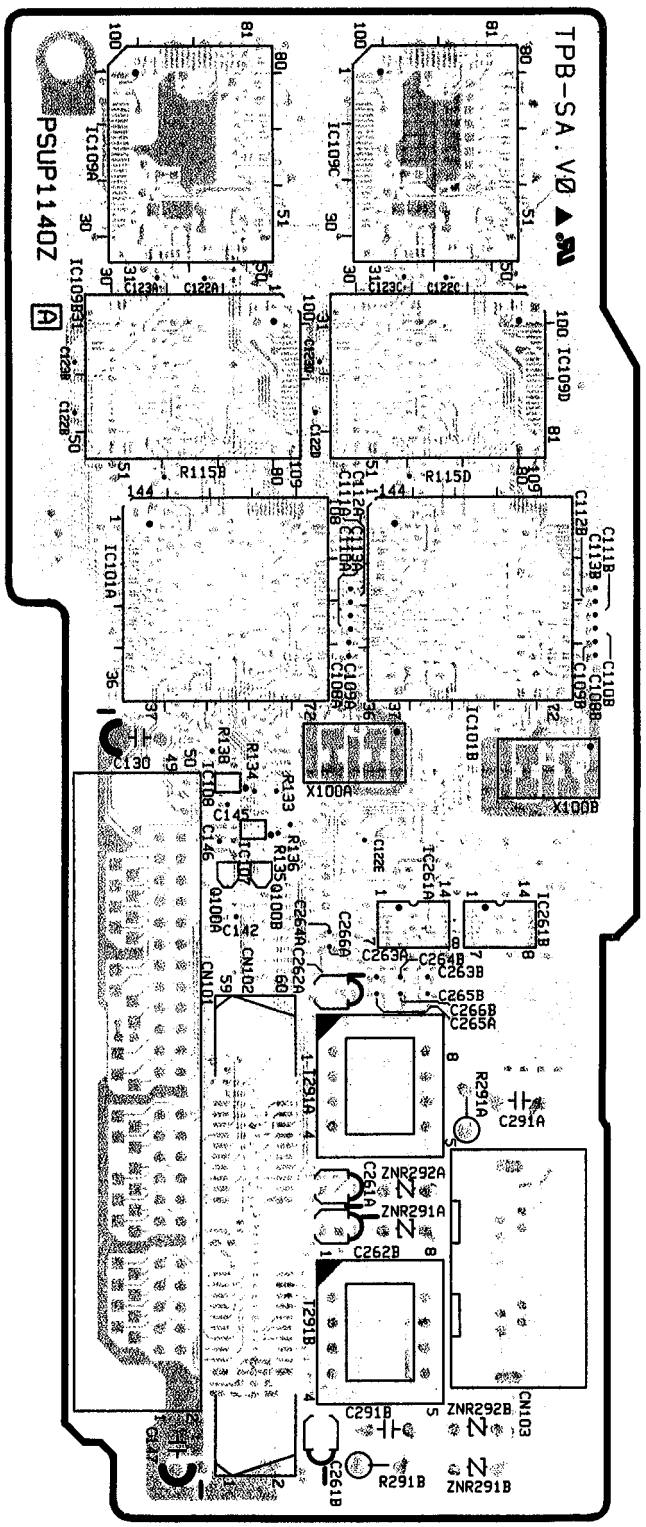



CN101
-5V
+5V
GND
-5VA
+5VA
VDD
HOST I/F (50P)
TO CPU SLOT
IC102 LS244
IC103 LS244
LS245 IC104
IC107
IC105 LS241
IC108
DSP G/A (B)
144-FQFP
IC101B COL-ASIC (CH3, CH4)
MODE1B
X1008
16.384MHz
Q100B
DTC143EU
DSPCLK
DCLK
SYNCN
4MHZ
SDENNB
SDENNA
RSTN
DVCN
DVDN
DPDN
UPDN
LINTN
PHWENNB
INT0B
LUVDNB
LUVANB
LUVCNB
VHWENNB

IAGRAM (KX-TVS204)



(COMPONENT VIEW)



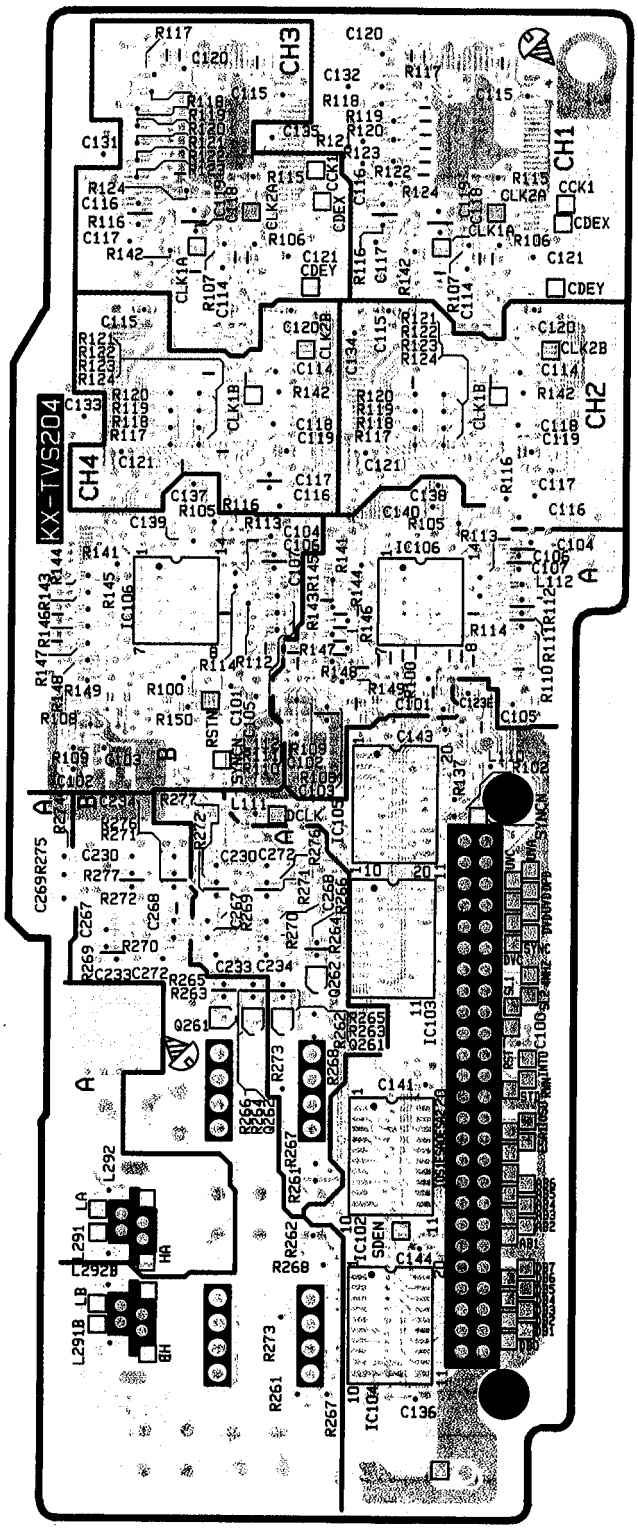
Notes:

1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3. The deve

OARD (KX-TVS204)

7 8 9 10 11 12

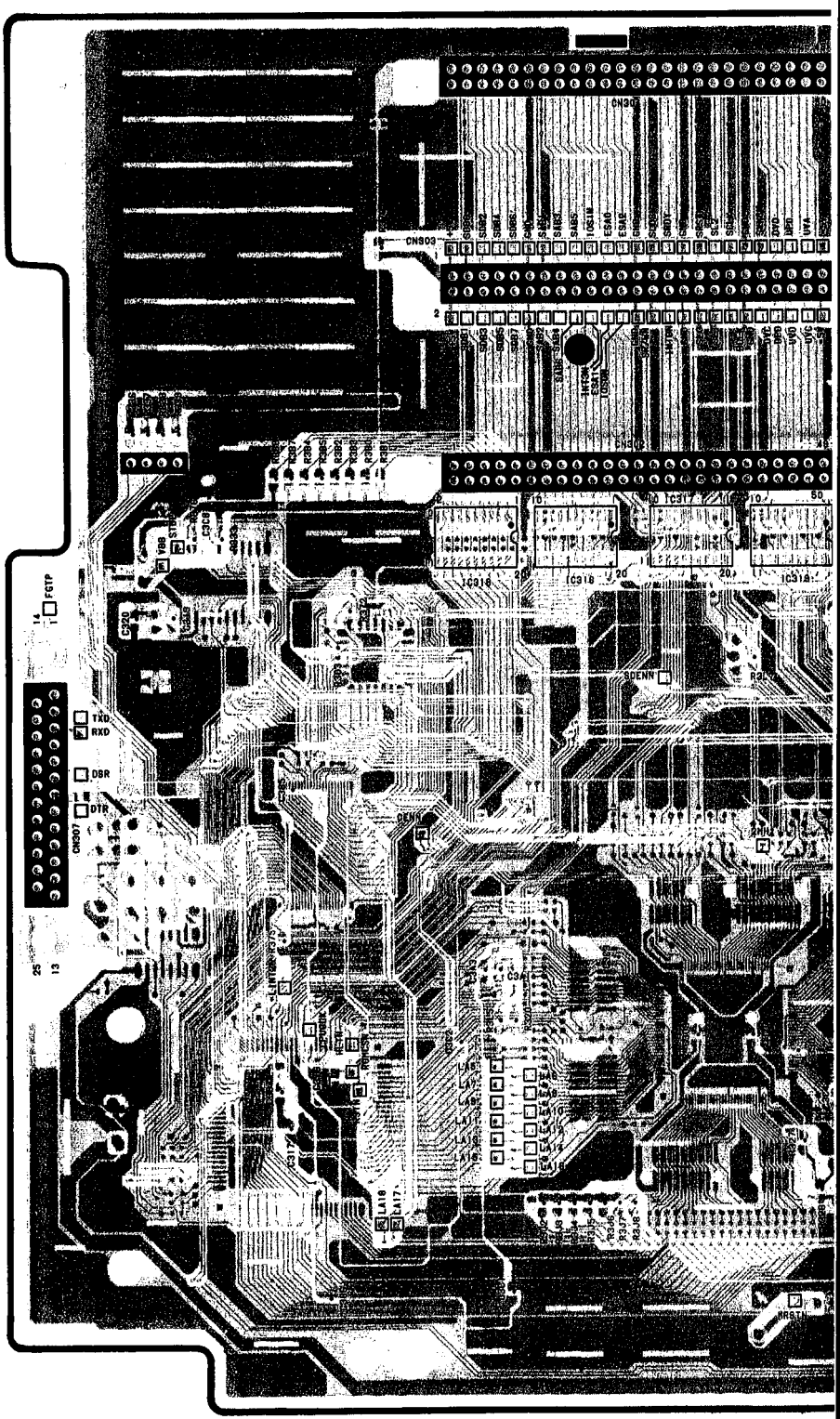
(BOTTOM VIEW)



3. The circuit board may be modified at any time with the development of new technology.

PRINTED CIRCUIT I

(BOTT



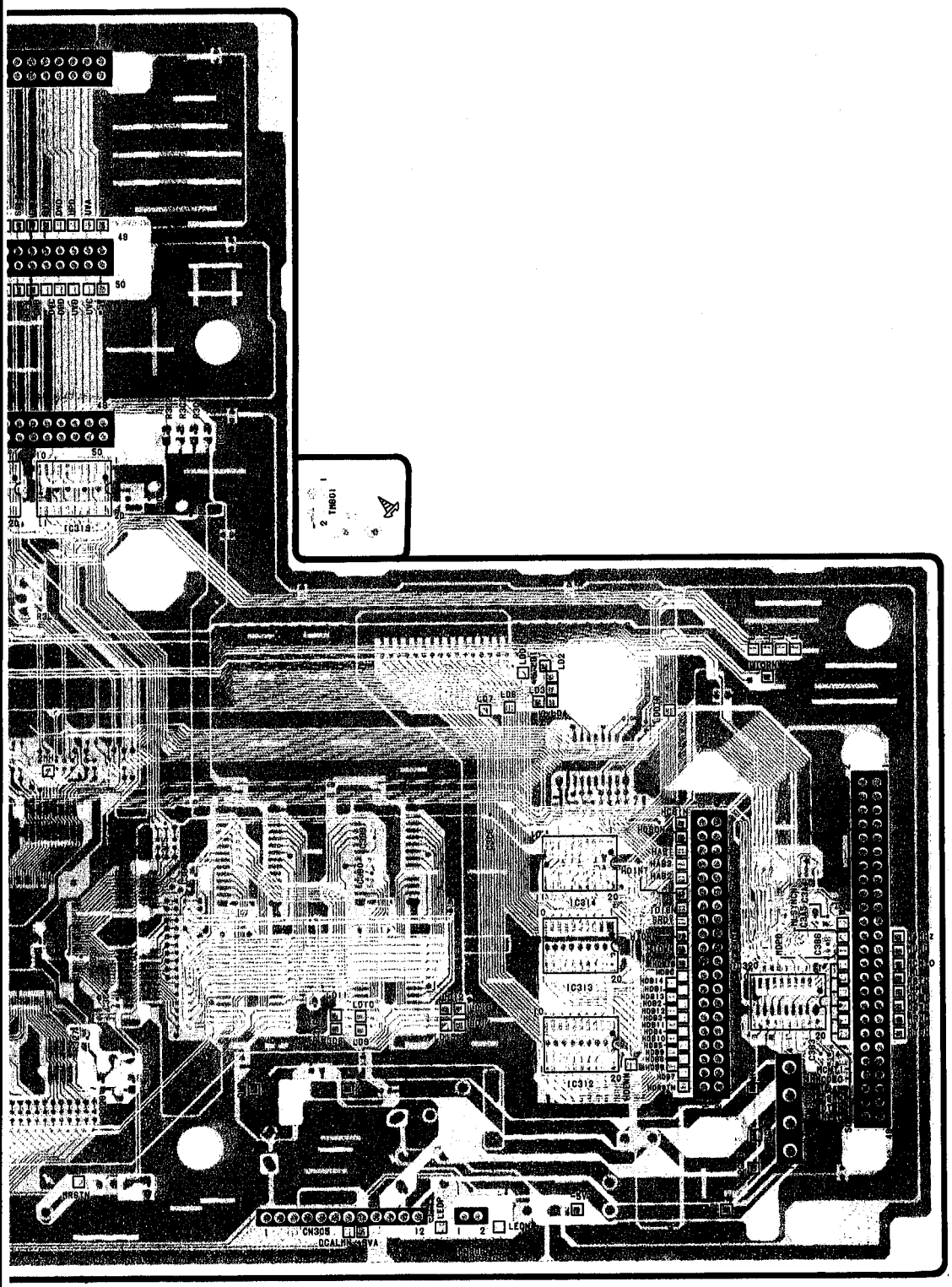
Notes:

1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3.

RCUIT BOARD (CPU)

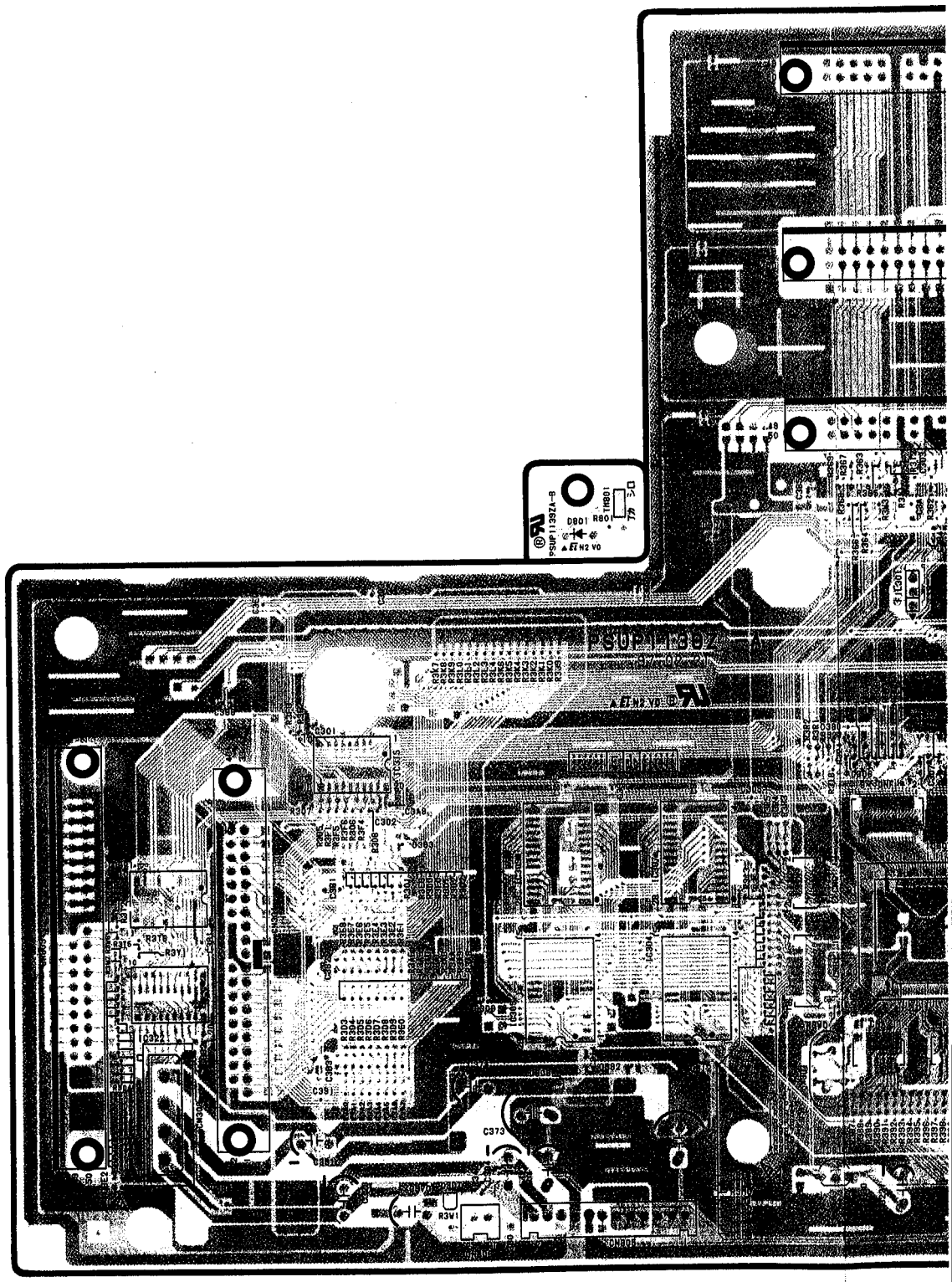
7 8 9 10 11 12

(BOTTOM VIEW)



cates 3. The circuit board may be modified at any time with the
lit development of new technology.

(COMPONENT VIE



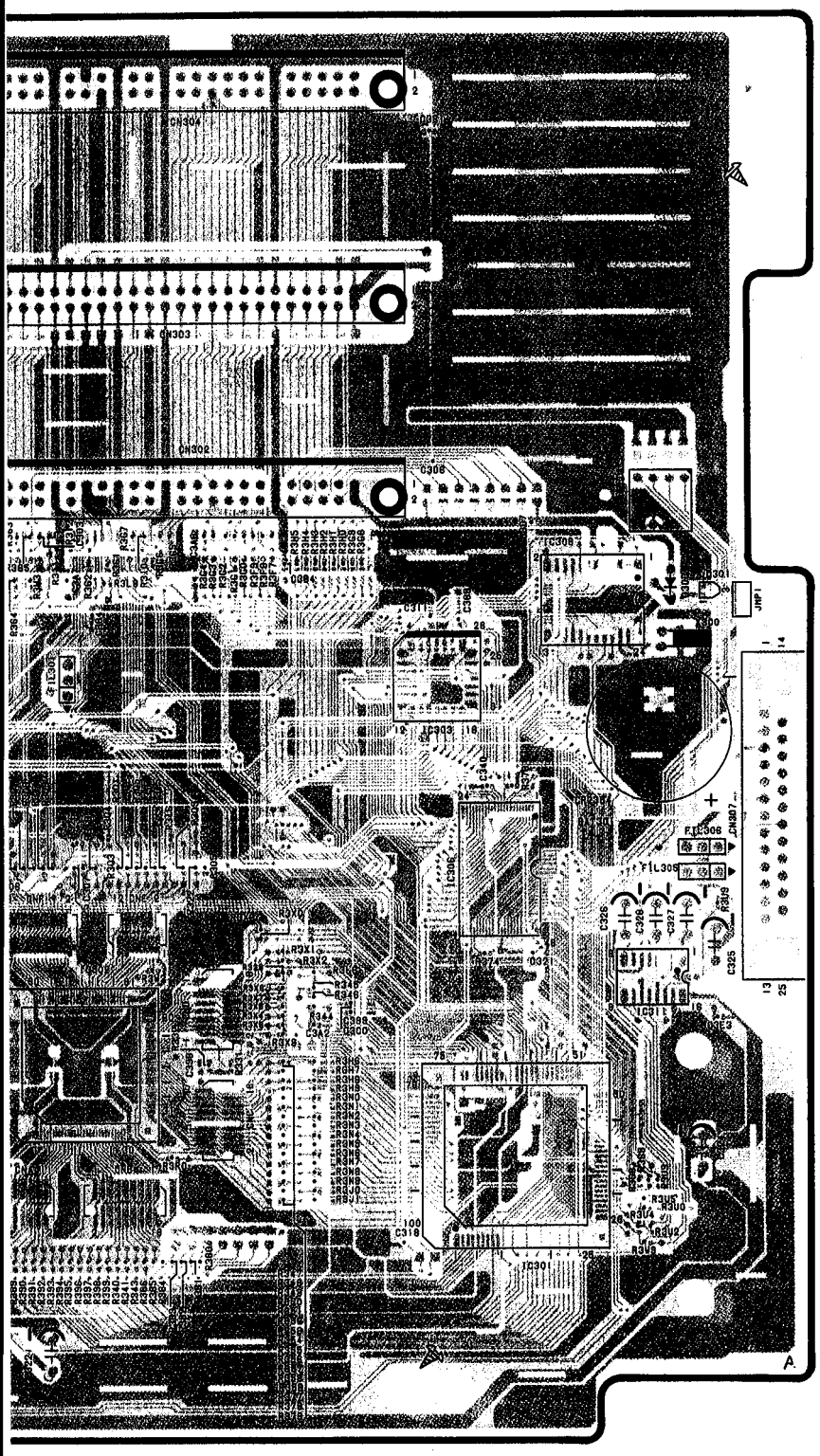
Notes:

1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3. The cir
develo

UIT BOARD (CPU)

7 | 8 | 9 | 10 | 11 | 12

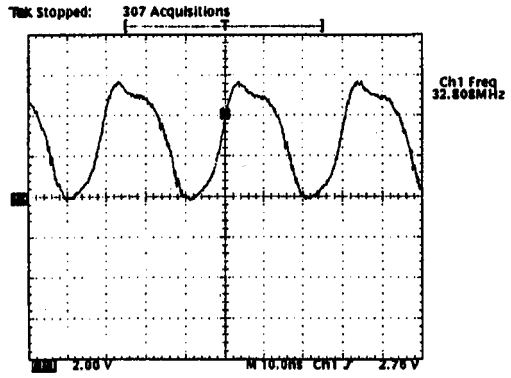
NENT VIEW)



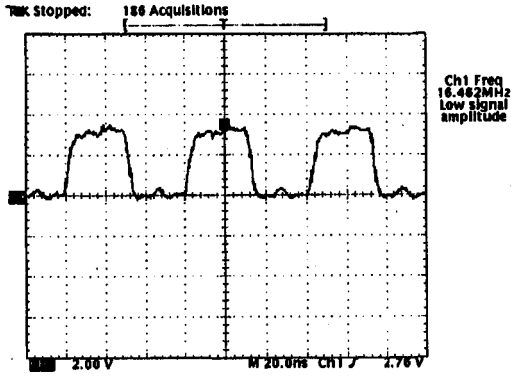
. The circuit board may be modified at any time with the development of new technology.

(Waveform of CPU Card)

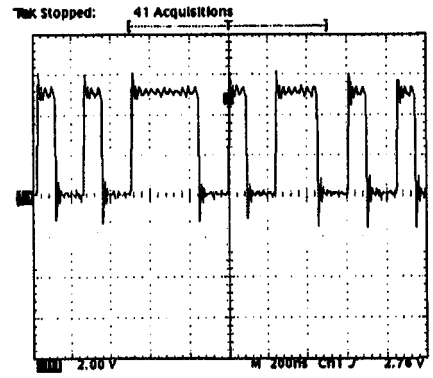
① XOUT



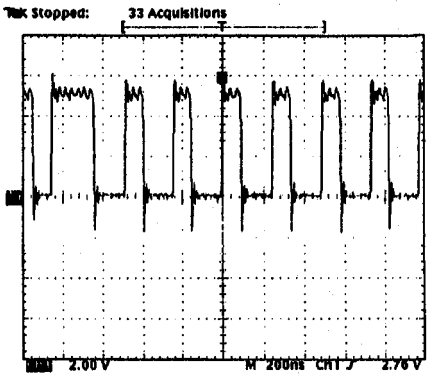
② CPU CLK



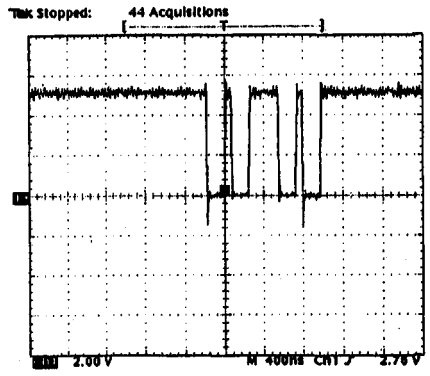
③ UDSN



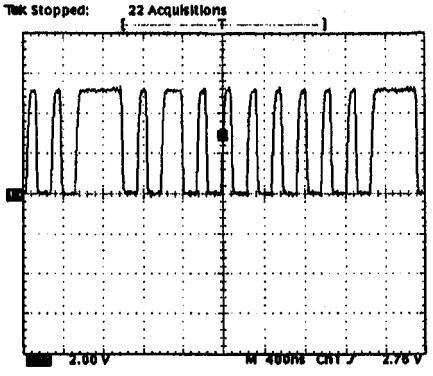
④ LDSN



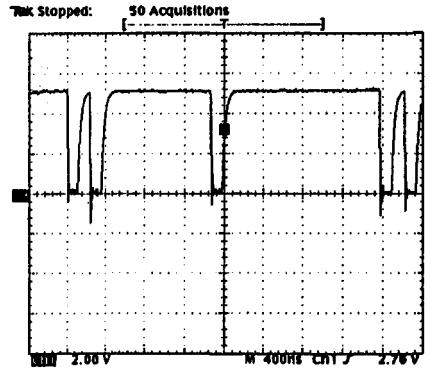
⑤ R/WN



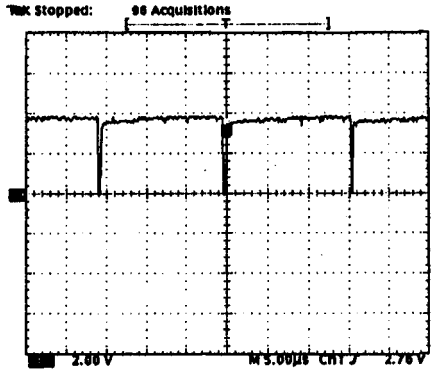
⑥ ASN



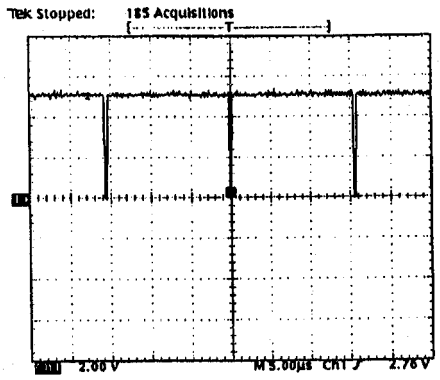
⑦ DAKN



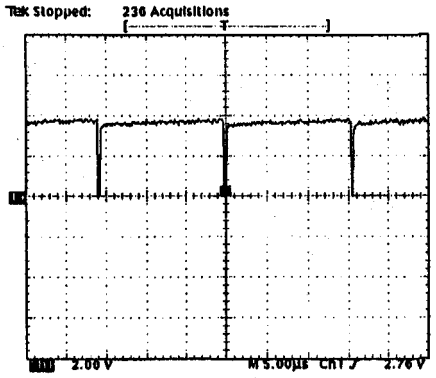
⑧ BRON



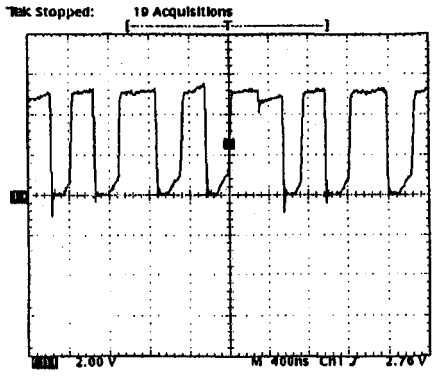
⑨ BGTN



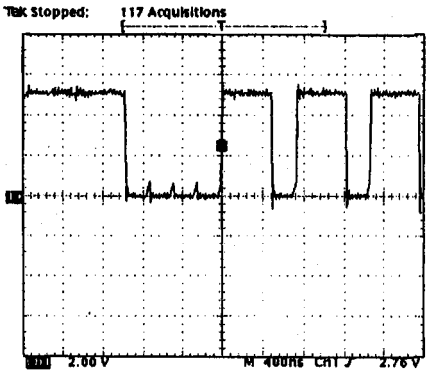
⑩ BAKN



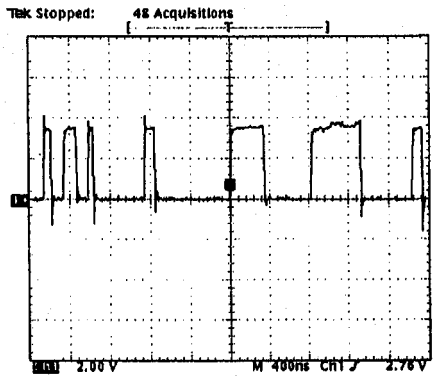
⑪ D0~D15



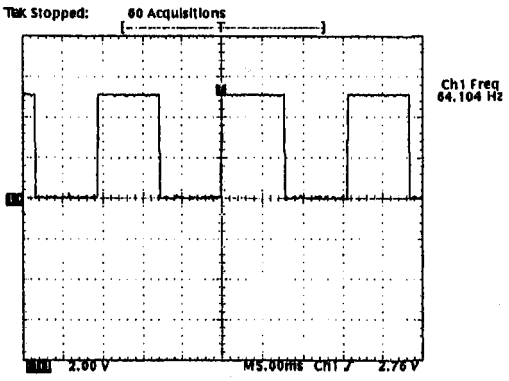
⑫ A0~A23



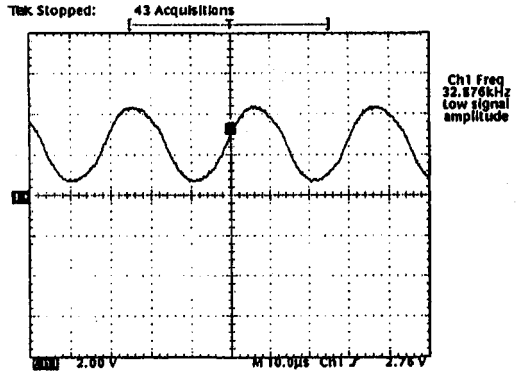
⑬ MA0~MA9



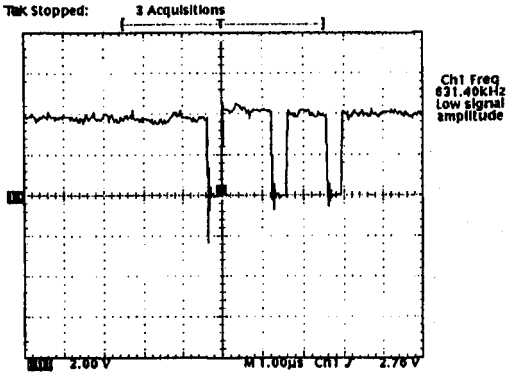
⑭ STDP



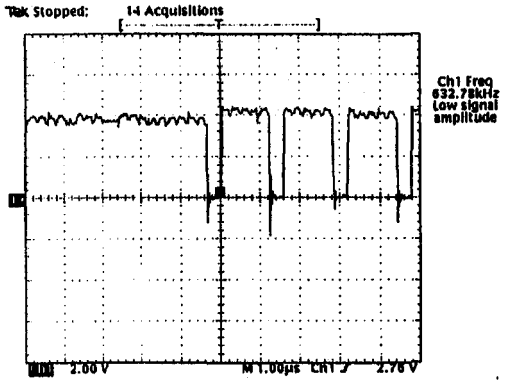
⑮ XT



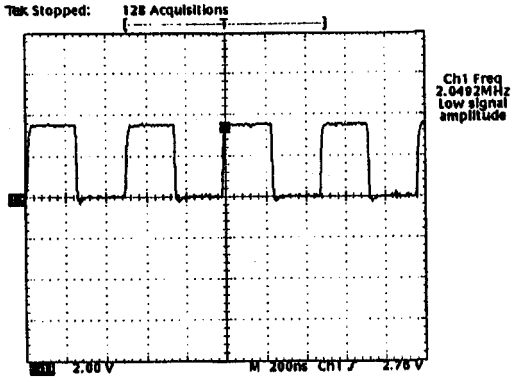
⑯ RTCSN



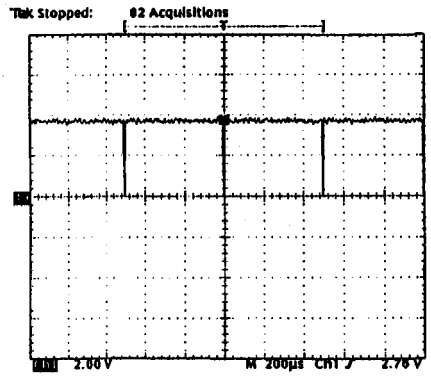
⑰ HDLCSN



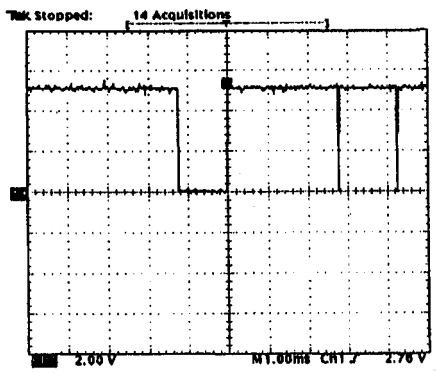
⑱ 2MHz



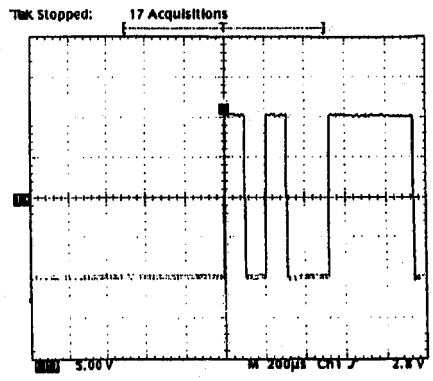
⑲ CENN



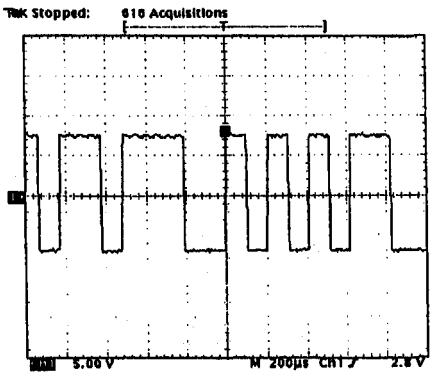
⑳ DPINTN



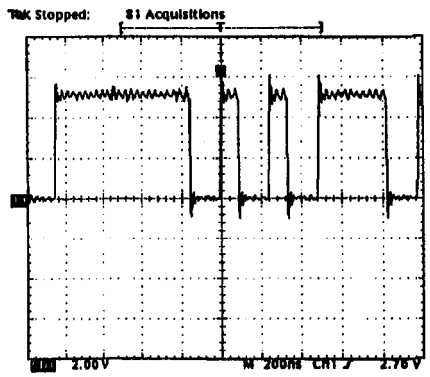
㉑ RXD



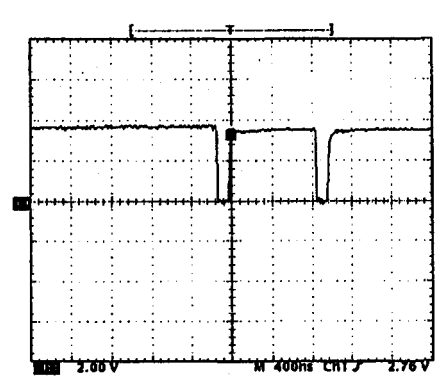
㉒ TXD



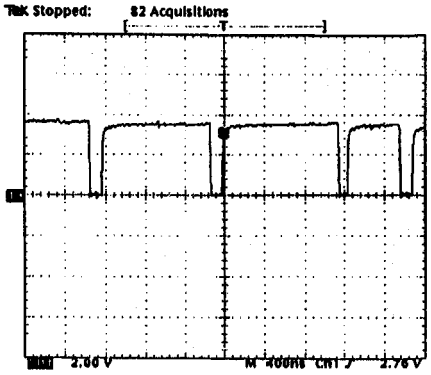
㉓ ROMCSN



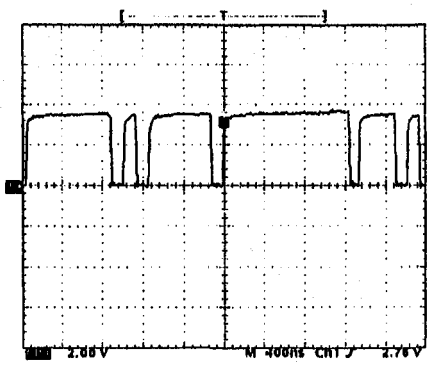
㉔ RASON



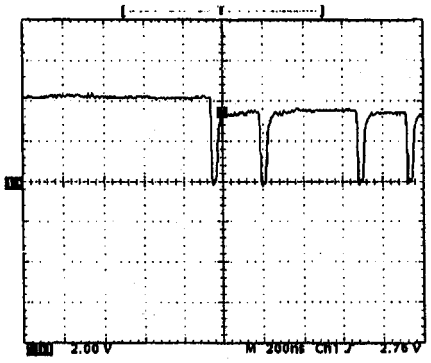
㉕ RASIN



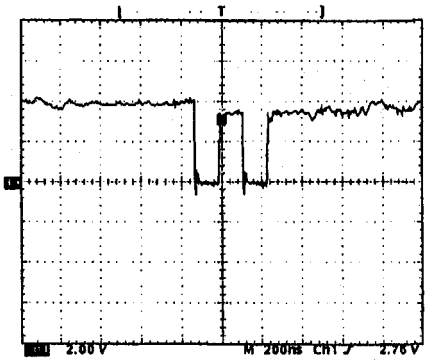
㉖ CASN



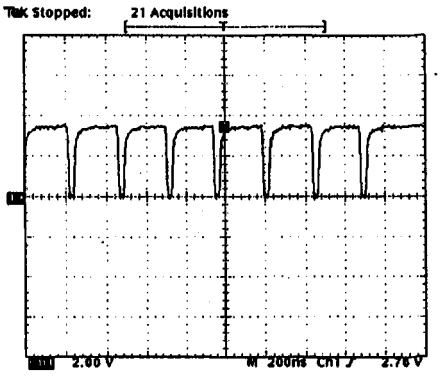
㉗ UWEN



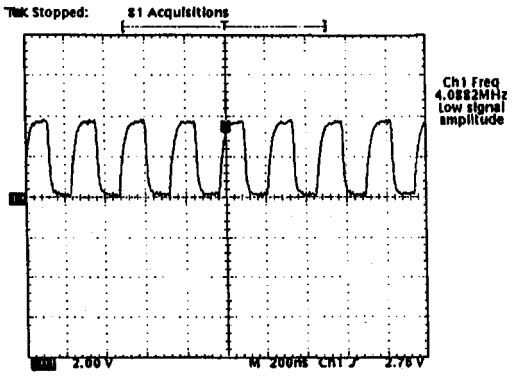
㉘ MOEN



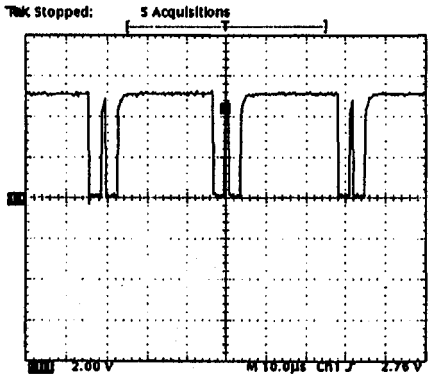
㉙ LWEN



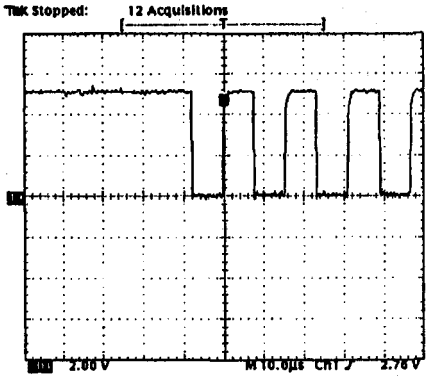
㉚ BCLK



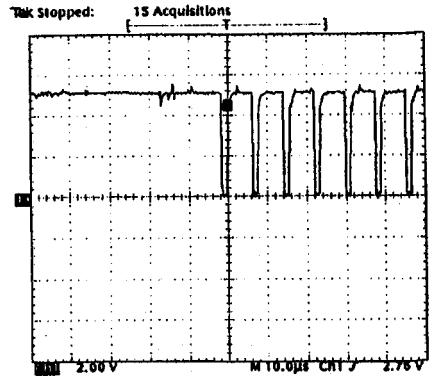
㉛ UPDN



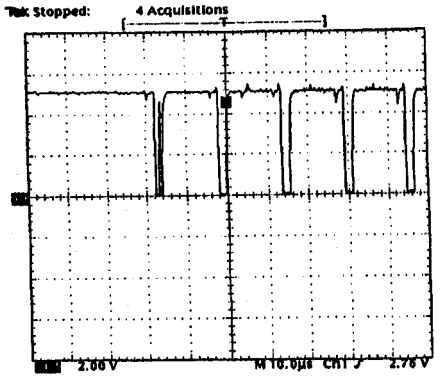
㉜ UVDN



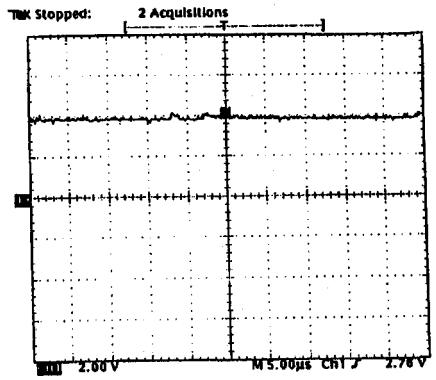
㉝ UVAN



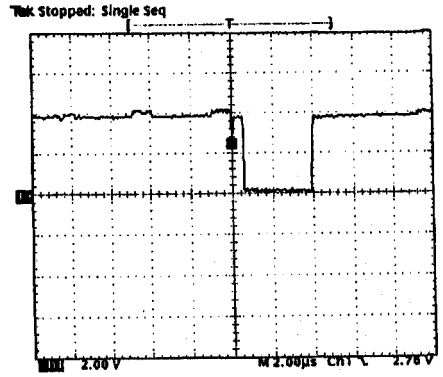
㉞ UVCN



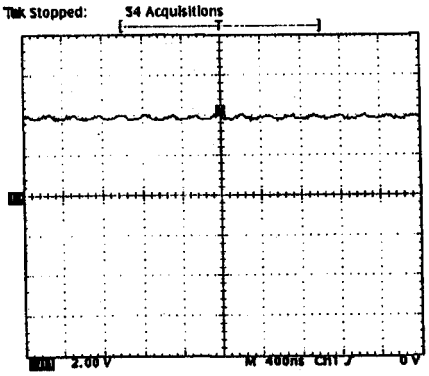
㉟ DPDN



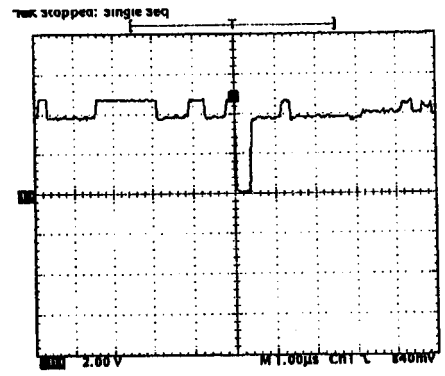
㊱ DVDN



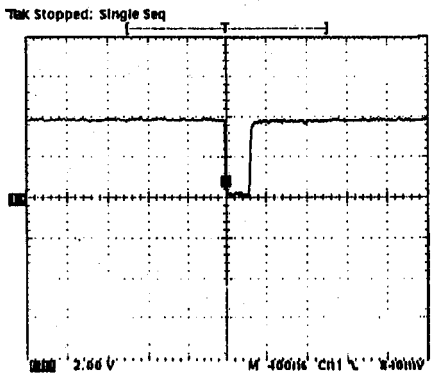
㊲ DVCN



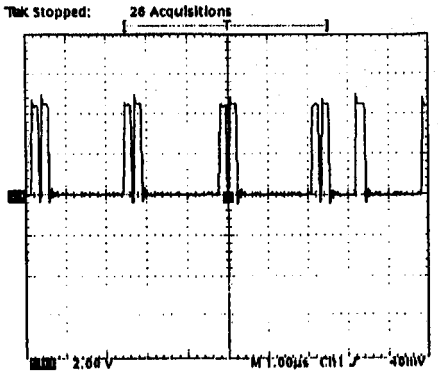
㊳ IOSON



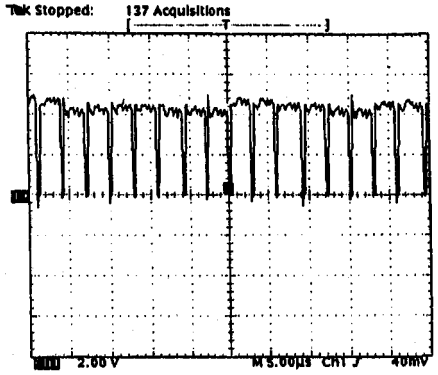
㊴ SYNCN

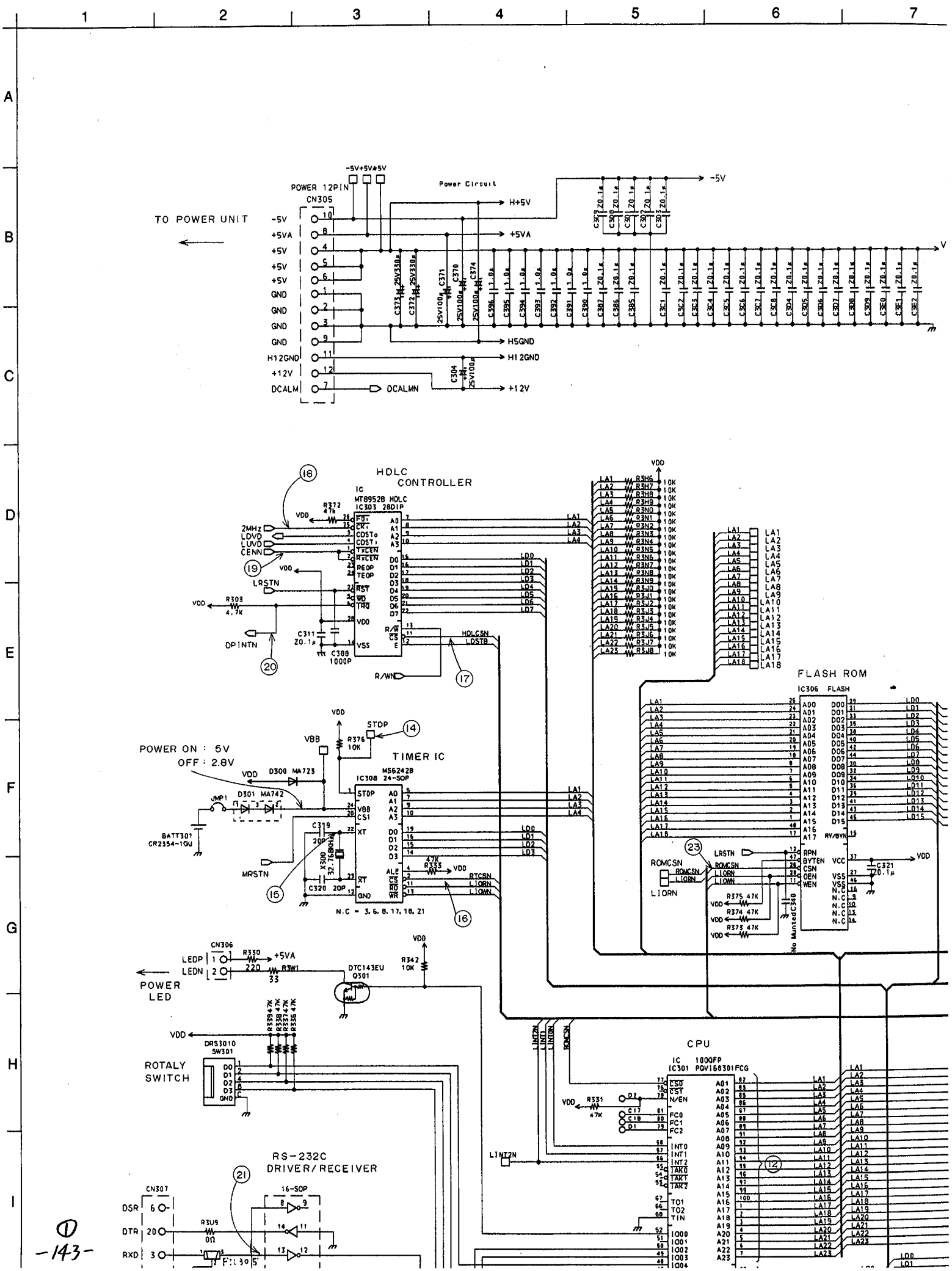


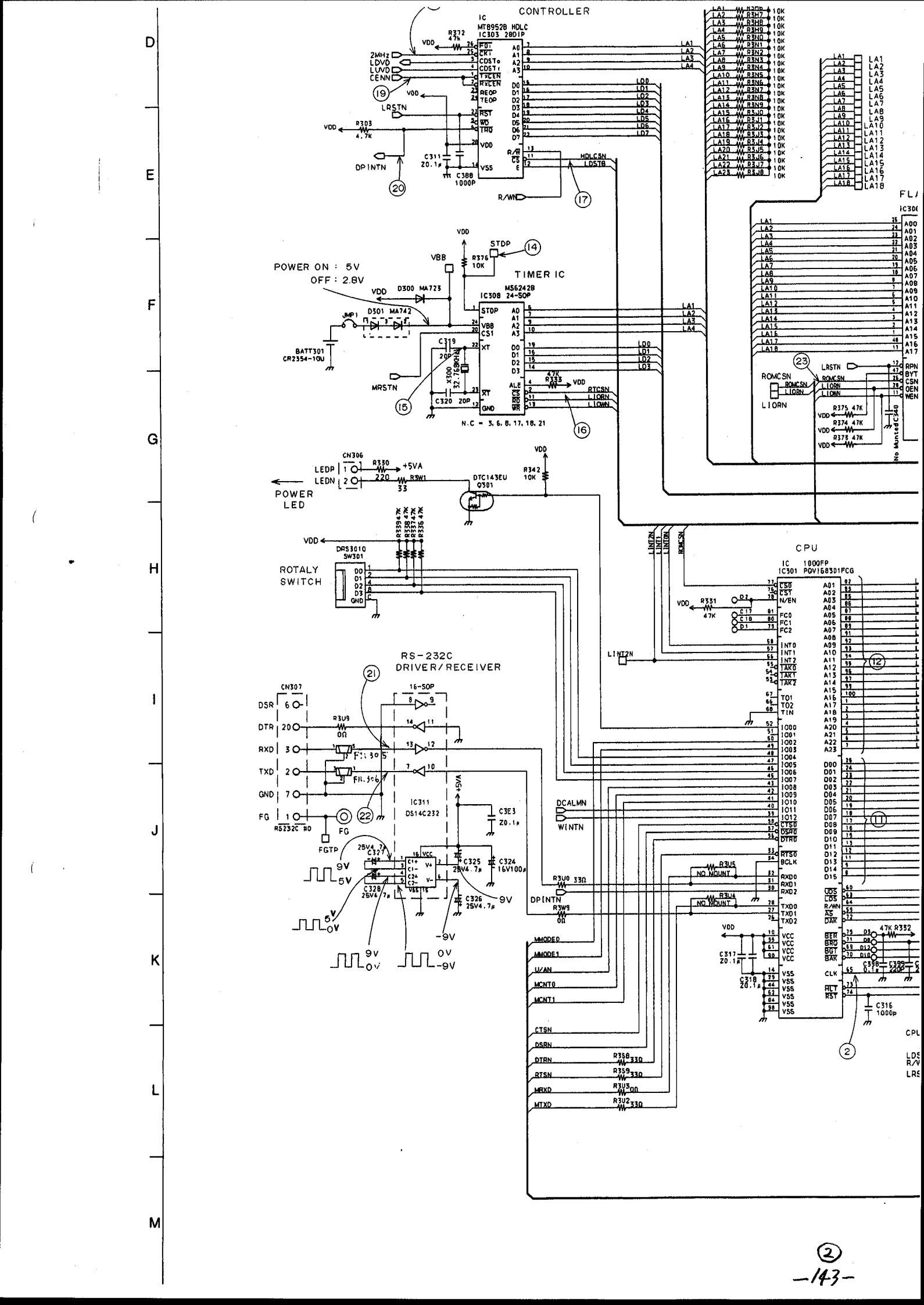
㊵ LDDIR



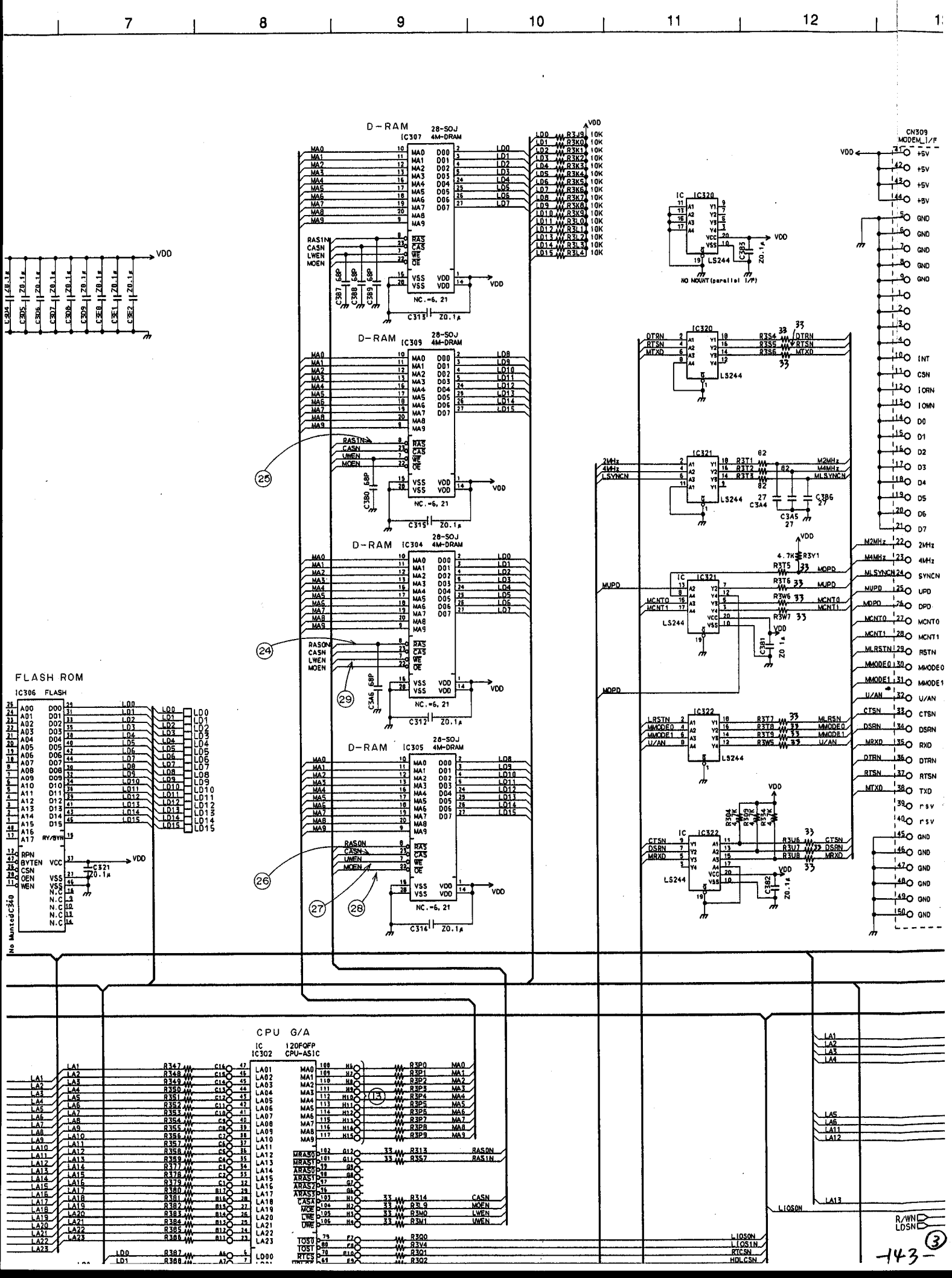
㊶ HDENN

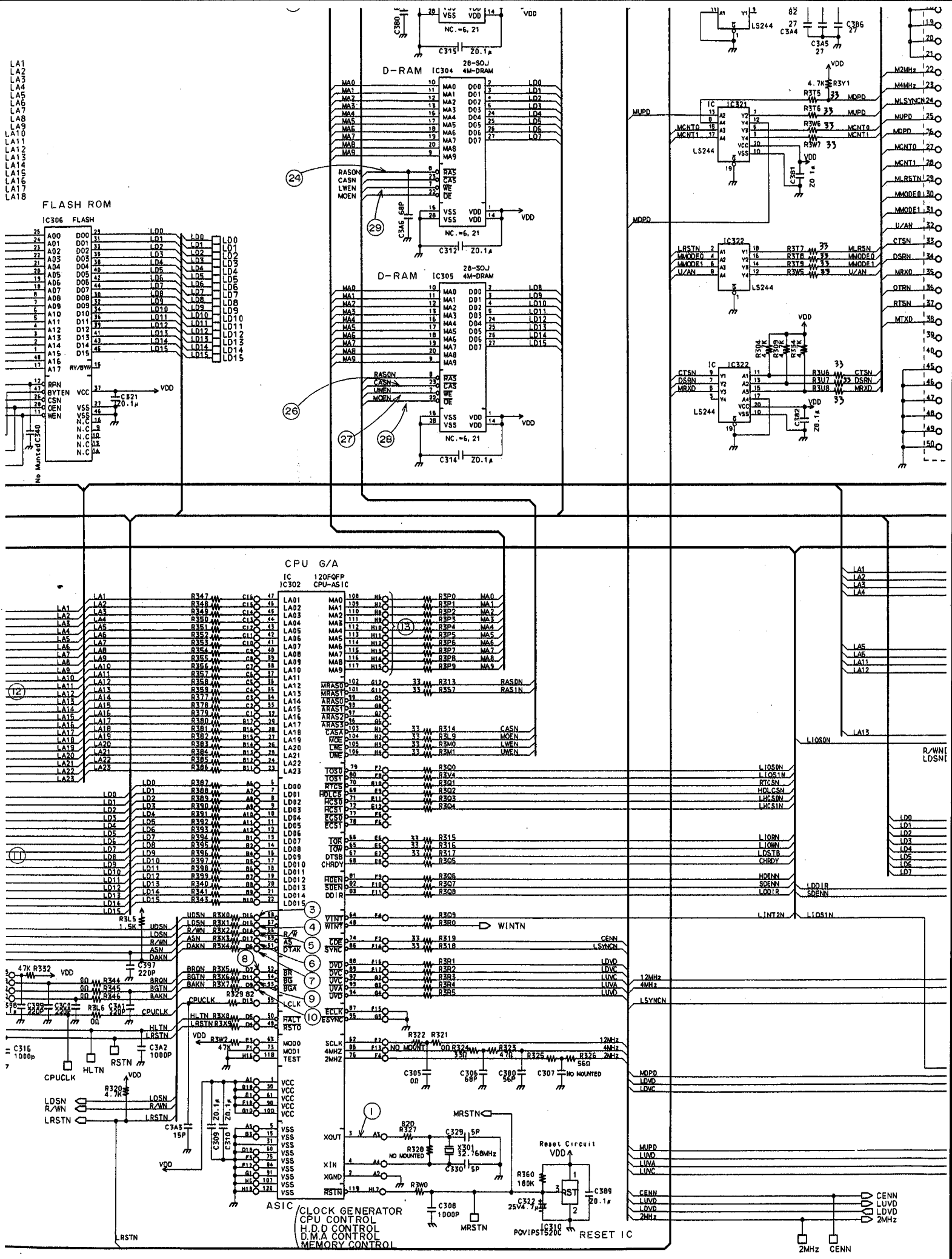


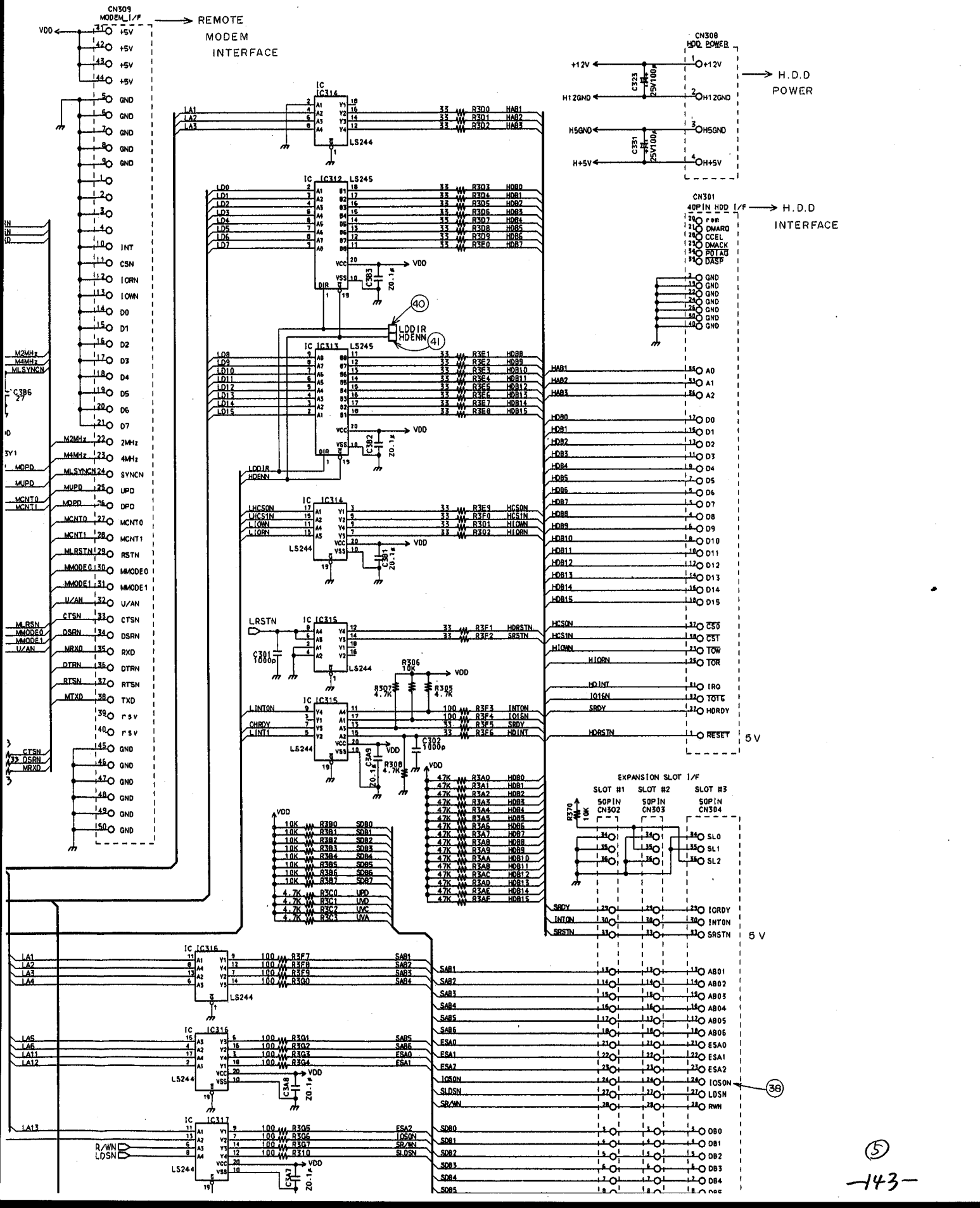

1
2
3
4
5
6
7
A
B
C
D
E
F
G
H
I
TO POWER UNIT
POWER 12PIN
CN305
-5V+5V+5V
Power Circuit
-5V
+5V
+5V
+5V
GND
GND
GND
GND
H12GND
+12V
DCALM
H+5V
+5VA
H5GND
H12GND
+12V
DCALMN
HDLC
CONTROLLER
IC
MT8952B HDLC
IC303 28DIP
2MHz
LDVD
LUVD
CENN
LRSTN
DPINTN
R/WN
HDLCSN
LDSTB
FLASH ROM
IC306 FLASH
ROMCSN
LIORN
TIMER IC
MS6242B
IC308 24-SOP
POWER ON : 5V
OFF : 2.8V
STDP
MRSTN
BATT301
CR2354-1GU
N.C = 3, 6, 8, 17, 18, 21
POWER
LED
LEDP
LEDN
DTC143EU
Q301
ROTALY
SWITCH
DRS3010
SW301
CPU
IC 100QFP
IC301 PQV168301FCG
LINT2N
RS-232C
DRIVER/RECEIVER
CN307
16-SOP
DSR
DTR
RXD
No Mounted C340
(1)
-143-

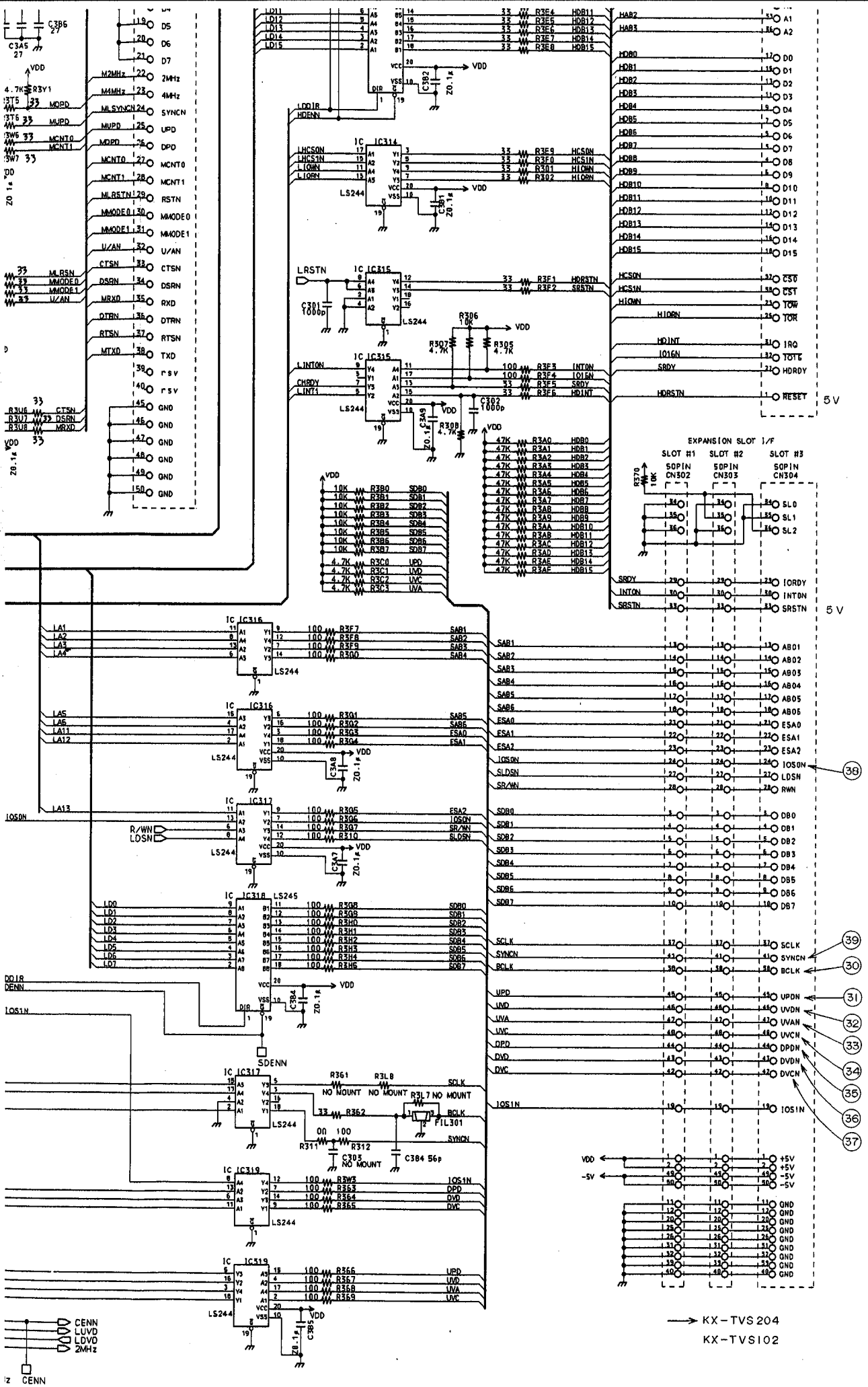

CONTROLLER
IC
MT8952B HDLC
IC303 28DIP
R372 4.7K
VDD
2MHz
LDVD
LUVD
CENN
LRSTN
R303 4.7K
DPINTN
C311 20.1μ
C388 1000P
HDLCSN
LDSTB
R/WN
LA1
LA2
LA3
LA4
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
10K
POWER ON : 5V
OFF : 2.8V
TIMER IC
MS6242B
IC308 24-SOP
STDP
R376 10K
VBB
D300 MA723
D301 MA742
JMP1
BATT301
CR2354-1GU
C319 20P
X300 32.768KHz
C320 20P
MRSTN
RTCSN
LIORN
LIOWN
R333 47K
N.C = 3, 6, 8, 17, 18, 21
ROMCSN
LRSTN
R375 47K
R374 47K
R375 47K
No Mounted C340
CN306
LEDP
LEDN
R330 220
R3W1 33
+5VA
POWER LED
DTC143EU
Q301
R342 10K
DRS3010
SW301
ROTALY SWITCH
R339 47K
R338 47K
R337 47K
R336 47K
CPU
IC 1000FP
IC301 PQV168301FCG
R331 47K
LINT2N
RS-232C
DRIVER/RECEIVER
CN307
DSR
DTR
RXD
TXD
GND
FG
R3U9 0Ω
FIL305
FIL306
16-SOP
IC311
DS14C232
RS232C RD
FGTP
C327 25V4.7μ
C325 25V4.7μ
C324 16V100μ
C328 25V4.7μ
C326 25V4.7μ
C3E3 Z0.1μ
9V
5V
0V
-9V
DCALMN
WINTN
DPINTN
R3U0 330Ω
R3U5 NO MOUNT
R3U4 NO MOUNT
R3W9 0Ω
MMODE0
MMODE1
U/AN
MCNT0
MCNT1
CTSN
DSRN
DTRN
RTSN
MRXD
MTXD
R358 330
R359 330
R3U3 0Ω
R3U2 330
C317 Z0.1μ
C318 Z0.1μ
C316 1000P
47K R332
C398 0.1μ
C399 220P
CPU
LDS
R/W
LRS

SCHEMATIC DIAGRAM (CPU)

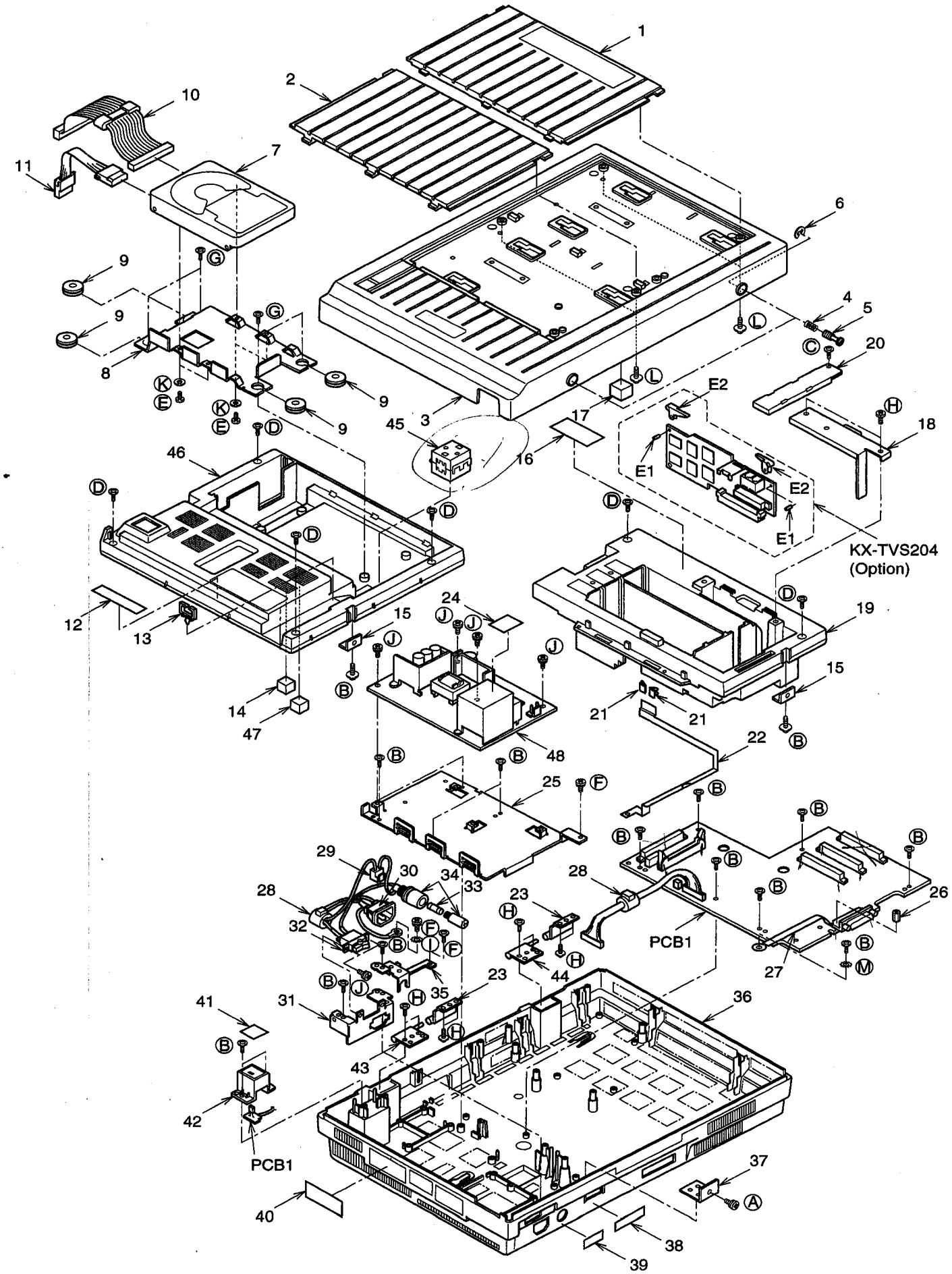



FLASH ROM
IC306 FLASH
D-RAM IC304 28-SOJ 4M-DRAM
D-RAM IC305 28-SOJ 4M-DRAM
IC IC321
IC IC322
LS244
CPU G/A
IC IC302 120FQFP CPU-ASIC
ASIC
CLOCK GENERATOR
CPU CONTROL
H.D.D CONTROL
D.M.A CONTROL
MEMORY CONTROL
Reset Circuit
IC310 PQVIPST520C RESET IC
X301 32.768MHz
WINTN
MRSTN
RASON
CASN
LWEN
UWEN
CENN
LSYNCN
LDVD
LDVC
LUVD
LUVC
LUVA
MUPD
MDPD
MCNT0
MCNT1
MLRSTN
MMODE0
MMODE1
U/AN
CTSN
DSRN
MRXD
DTRN
RTSN
MTXD
LIOSON
LIOS1N
RTCSN
HDLCSN
LHCSON
LHCS1N
LIORN
LIOWN
LDSTB
CHRDY
HDENN
SDENN
LDDIR
LINT2N
LIOS1N
R/WN
LDSN
LRSTN
HLTN
CPUCLK
12MHz
4MHz
2MHz

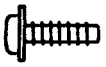
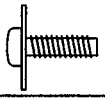
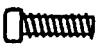

CN309
MODEM I/F
REMOTE
MODEM
INTERFACE
CN308
HDD POWER
H.D.D
POWER
CN301
40PIN HDD I/F
H.D.D
INTERFACE
IC314
IC312 LS245
IC313 LS245
IC315
IC316
IC317
LS244
LDDIR
HDENN
EXPANSION SLOT I/F
SLOT #1
SLOT #2
SLOT #3
5V


EXPANSION SLOT I/F
SLOT #1
SLOT #2
SLOT #3
50PIN CN302
50PIN CN303
50PIN CN304
5V
KX-TVS204
KX-TVS102

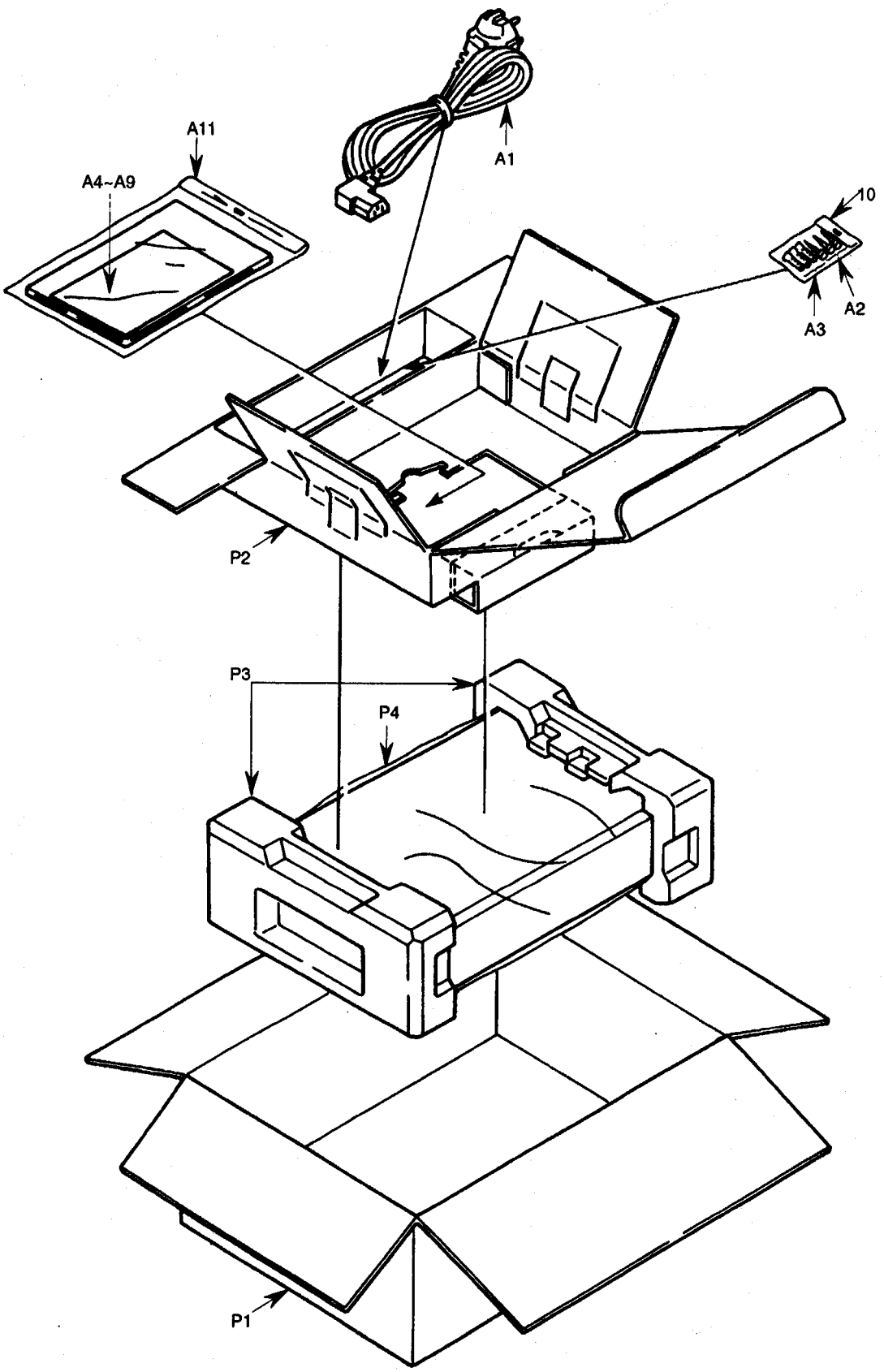
CABINET AND ELECTRICAL PARTS LOCATION



ACTUAL SIZE OF SCREWS AND WASHER

Ref. No.	Part No.	Figure
Ⓐ	XSN4D8FN	
Ⓑ	XTW3+S10P	
Ⓒ	XYN3+F8FN	
Ⓓ	XTW3+S16M	
Ⓔ	XSN6X32+6	
Ⓕ	XYN4+C8	
Ⓖ	PJYC3+MC12	
Ⓗ	XTB3+10GFN	
Ⓘ	XWC4B	
Ⓙ	XYN3+C6	
Ⓚ	XWA35B	
Ⓛ	XTW3+W8F	
Ⓜ	XWC3B	

ACCESSORIES AND PACKING MATERIALS



This replacement parts list is for KX-TVS200 only. Refer to the simplified manual (cover) for other areas.

REPLACEMENT PARTS LIST
Model KX-TVS200

Notes:
1. The marking (RTL) indicates that the Retention Time is limited for this item. After the discontinuation of this assembly in production, the item will continue to be available for a specific period of time. The retention period of availability is dependent on the type of assembly, and in accordance with the laws governing part and product retention. After the end of this period, the assembly will no longer be available.
2. Important safety notice.
   Components identified by the ⚠ mark special characteristics important for safety.
   When replacing any of these components, use only manufacturer's specified parts.
3. The S mark indicates service standard parts and may differ from production parts.
4. RESISTORS & CAPACITORS
   Unless otherwise specified.
   All resistors are in ohms (Ω) k=1000Ω, M=1000kΩ
   All capacitors are in MICRO FARADS(μF) P= μμF
   *Type &Wattage of Resistor

Type

ERC:Solid	ERX:Metal Film	PQRD:Carbon
ERD:Carbon	ERG:Metal Oxide	PQRQ:Fuse
PQ4R:Chip	ERO:Metal Film	ERF:Wire Wound

Wattage

10,16,18:1/8W	14,25,S2:1/4W	12,50,S1:1/2W	1:1W	2:2W	5:5W

ECFD:Semi-Conductor	ECCD,ECKD,PQCBC,PQVP : Ceramic
ECQS:Styrol	ECQM,ECQV,ECQE,ECQU,ECQB : Polyester
PQCBX,ECUV:Chip	ECEA,ECSZ,ECOS : Electrolytic
ECMS:Mica	ECQP : Polypropylene

Voltage

ECQ Type	ECQG ECQV Type	ECSZ Type	Others	
1H: 50V	05: 50V	OF:3.15V	OJ :6.3V	1V :35V
2A:100V	1:100V	1A:10V	1A :10V	50,1H:50V
2E:250V	2:200V	1V:35V	1C :16V	1J :63V
2H:500V		OJ:6.3V	1E,25:25V	2A :100V

	Part No.	Part Name & Description	Pcs
		CABINET & ELECTRICAL PARTS	
1	PQKV10006C1	COVER	1
2	PQKV10005U1	COVER	1
3	PQKE10021L1	COVER	1
4	PQUS141Z	SPRING	2
5	PQHD10011X	SCREW	2
6	XUC3VW	RETAINING RING	2
7	PSWETVS200M	HEAD DISK DRIVE UNIT	1
8	PSMH1093Z	FRAME, HDD	1
9	PSHG1094Z	RUBBER PARTS, SPACER	4
10	PSJS40R88Z	CONNECTOR, 40P	1
11	PSJS04R87Z	CONNECTOR, 4P	1
12	PSQT1026Z	INDICATION LABEL	1
13	PQHR118Z	CLAMPER	1
14	PSHG1111Z	RUBBER PARTS, SPACER	1
15	PQMH10008Z	ANGLE	2
16	PQQT10918Z	INDICATION LABEL	1
17	PSHG1064Z	RUBBER PARTS, SPACER	1
18	PSMD1010Z	ANGLE	1
19	PQKE10037U1	PARTING PLATE	1
20	PSMD1011Z	ANGLE	1
21	PQMH10152Z	SPRING	2
22	PQMC10101Z	MAGNETIC SHIELD PLATE	1
23	PQMH10009Z	HINGE	2
24	PSQT1308Z	INDICATION LABEL	1
25	PSMH1104Z	FRAME, POWER CARD	1
26	PQHE7011Z	NUT	1
27	PSWW1001Z	LEAD WIRE	1
28	PQLB5D2	FERRITE CORE	2
29	PSJS02R91Z	CONNECTOR, 2P	1
30	PQJP3A3Z	AC INLET ⚠	1
31	PQMH10027Y	CHASSIS	1
32	EST15304T	SWITCH, POWER ⚠	1
33	XBA2C25ND1L	FUSE ⚠	1
34	PQJV5Z	FUSE HOLDER ⚠	1
35	PSMH1043Z	ANGLE	1
36	PQKM10086F1	CABINET BODY	1
37	PQMC10059Y	MAGNETIC SHIELD PLATE	1
38	PSQT1314Z	INDICATION LABEL	1
39	PSQT1277Z	INDICATION LABEL	1
40	PSGT1356Z	NAME PLATE	1
41	PQGP10009Z1	PANEL	1
42	PQGG10009Z1	GRILLE	1
43	PQMH10010Y	HINGE	1
44	PQMH10010Z	HINGE	1
45	PSLB5F2	FERRITE CORE	1
46	PQKF10066U1	UPPER CABINET	1
47	PSHG1112Z	RUBBER PARTS, SPACER	1
48	PSLP1047Z	POWER CARD (RTL) ⚠	1
		ACCESSORIES AND PACKING MATERIALS	
A1	PQJA10016Z	POWER CORD, AC ⚠	1
A2	PQHE5008Z	MOUNTING BRACKET, SCREW	3
A3	PQHE10Z	MOUNTING BRACKET, PLUG	3
A4	PSQX1215Z	INSTALLATION MANUAL	1
A5	PSQX1237Z	FRONT COVER FOR I/M	1
A6	PSQX1238Z	BACK COVER FOR I/M	1
A7	PSQX1221Z	SUBSCRIBER'S GUIDE	1
A8	PQQX10552W	TEMPLATE	1
A9	PQQX10970Y	REMOTE LEAFLET	1
A10	XZB05X08A03	BAG,POLYETHYLENE	1
A11	XZB30X40A04	BAG,POLYETHYLENE	1
P1	PSPK1248Z	PACKING CASE	1
P2	PQPN10191Y	ACCESSORY BOX	1
P3	PQPN10196Y	CUSHION	2
P4	PQPP10022Z	BAG,POLYETHYLENE	1
		CPU CARD PARTS	
PCB1	PSWPTVS200M	CPU CARD ASS'Y (RTL)	1
IC301	PSVI68301FGG	IC	1
IC302	PQVIPD656109	IC	1
IC303	PSVIMT8952BP	IC	1
IC304,305	PSVIHM5148CE	IC	2
IC306	PSWITVS200M	IC (ROM)	1
IC307	PSVIHM5148CE	IC	1
IC308	PQVIMS6242BG	IC	1
IC309	PSVIHM5148CE	IC	1
IC310	PQVIPS520C	IC	1
IC311	PQVIDS14C232	IC	1
IC312,313	PQVISN7L245S	IC S	2
IC314,315	PQVISN7L244S	IC S	2
IC316,317	PQVISN7L244S	IC	2
IC318	PQVISN7L245S	IC S	1
IC319-322	PQVISN7L244S	IC S	4

This replacement parts list is for KX-TVS200 only. Refer to the simplified manual (cover) for other areas.

Ref. No.	Part No.	Part Name & Description		Pcs
		(TRANSISTOR)		
Q301	PQVTDTC143E	TRANSISTOR(SI)		1
		(DIODES)		
D300	MA723	DIODE(SI)		1
D301	MA742	DIODE(SI)		1
D801	LN242RP	DIODE(SI)	S	1
		(BATTERY)		
BAT301	CR23541GUF	LITHIUM BATTERY		1
		(CONNECTORS)		
CN301	PQJP40A09Z	CONNECTOR, 40P		1
CN302	PQJS50S33Z	CONNECTOR, 50P		1
CN303	PQJS50S33Z	CONNECTOR, 50P		1
CN304	PQJS50S33Z	CONNECTOR, 50P		1
CN305	PSJS12R89Y	CONNECTOR, 12P		1
CN306	PQJP2D70Z	CONNECTOR, 2P		1
CN307	PQJS25P31Z	SOCKET, 25P		1
CN308	PSJP04A46Z	CONNECTOR, 4P		1
CN309	PQJS50S33Z	CONNECTOR, 50P		1
TM801	PQJS02R48Y	CONNECTOR, 2P		1
		(CAPACITORS)		
C3A1	PQCUV1H221JC	220P	S	1
C3A2	ECUV1H102KBV	0.001	S	1
C3A3	PQCUV1H150JC	15P		1
C3A4	PQCUV1H270JC	27P		1
C3A5	PQCUV1H270JC	27P		1
C3A6	PQCUV1H680JC	68P		1
C3A7	ECUV1C104KBV	0.1	S	1
C3A8	ECUV1C104KBV	0.1	S	1
C3A9	ECUV1C104KBV	0.1	S	1
C3B0	PQCUV1H680JC	68P		1
C3B1	ECUV1C104KBV	0.1	S	1
C3B2	ECUV1C104KBV	0.1	S	1
C3B3	ECUV1C104KBV	0.1	S	1
C3B4	ECUV1C104KBV	0.1	S	1
C3B5	ECUV1C104KBV	0.1	S	1
C3B6	PQCUV1H270JC	27P		1
C3B7	PQCUV1H680JC	68P		1
C3B8	ECUV1H680JCV	68P		1
C3B9	PQCUV1H680JC	68P		1
C3C0	ECUV1H221JCV	220P	S	1
C3C1	PQCUV1H104ZF	0.1		1
C3C2	PQCUV1H104ZF	0.1		1
C3C3	PQCUV1H104ZF	0.1		1
C3C4	PQCUV1H104ZF	0.1		1
C3C5	PQCUV1H104ZF	0.1		1
C3C6	PQCUV1H104ZF	0.1		1
C3C7	PQCUV1H104ZF	0.1		1
C3C8	PQCUV1H104ZF	0.1		1
C3C9	ECUV1C104KBV	0.1	S	1
C3D0	ECUV1C104KBV	0.1	S	1
C3D1	ECUV1C104KBV	0.1	S	1
C3D2	ECUV1C104KBV	0.1	S	1
C3D3	ECUV1C104KBV	0.1	S	1
C3D4	ECUV1C104KBV	0.1	S	1
C3D5	ECUV1C104KBV	0.1	S	1
C3D6	ECUV1C104KBV	0.1	S	1
C3D7	ECUV1C104KBV	0.1	S	1
C3D8	ECUV1C104KBV	0.1	S	1
C3D9	ECUV1C104KBV	0.1	S	1

Ref. No.	Part No.	Part Name & Description		Pcs
C3E0	ECUV1C104KBV	0.1	S	1
C3E1	ECUV1C104KBV	0.1	S	1
C3E2	ECUV1C104KBV	0.1	S	1
C3E3	ECUV1C104KBV	0.1	S	1
C301,302	ECUV1H102KBV	0.001	S	2
C304	ECEA1EU101	100		1
C305	ERJ3GEY0R00	0		1
C306	ECUV1H680JCV	68P		1
C308	ECUV1H102KBV	0.001	S	1
C309	PQCUV1H104ZF	0.1		1
C310	PQCUV1H104ZF	0.1		1
C311-315	ECUV1C104KBV	0.1	S	5
C316	PQCUV1H102J	0.001	S	1
C317	PQCUV1H104ZF	0.1		1
C318	ECUV1C104KBV	0.1	S	1
C319	PQCUV1H200JC	20P		1
C320	PQCUV1H200JC	20P		1
C321	ECUV1C104KBV	0.1	S	1
C322	ECEA1VKS4R7	4.7	S	1
C323,324	ECEA1EU101	100		2
C325-328	ECEA1VKS4R7	4.7	S	4
C329	PQCUV1H5R0CC	5		1
C330	PQCUV1H5R0CC	5		1
C331	ECEA1EU101	100		1
C370,371	ECEA1EU101	100		2
C372,373	ECEA1EU331	330		2
C374	ECEA1EU101	100		1
C380	ECUV1H560JCV	56P		1
C381,382	ECUV1C104KBV	0.1	S	2
C383	PQCUV1H104ZF	0.1		1
C384	ECUV1H560JCV	56P		1
C385	PQCUV1H104ZF	0.1		1
C386	PQCUV1H104ZF	0.1		1
C387	PQCUV1H104ZF	0.1		1
C388	ECUV1H102KBV	0.001	S	1
C389	PQCUV1H104ZF	0.1		1
C390-396	PQCUV1H105JC	1	S	7
C397	PQCUV1H221JC	220P	S	1
C398	ECUV1C104KBV	0.1	S	1
C399	ECUV1H221JCV	220P	S	1
		(CERAMIC FILTERS)		
FIL301	PQVFTU50MT	CERAMIC FILTER		1
FIL305	PQVFTU50MT	CERAMIC FILTER		1
FIL306	PQVFTU50MT	CERAMIC FILTER		1
		(RESISTORS)		
C305	ERJ3GEY0R00	0		1
R3AA	ERJ3GEYJ473	47K		1
R3AB	ERJ3GEYJ473	47K		1
R3AC	ERJ3GEYJ473	47K		1
R3AD	ERJ3GEYJ473	47K		1
R3AE	ERJ3GEYJ473	47K		1
R3AF	ERJ3GEYJ473	47K		1
R3A0	ERJ3GEYJ473	47K		1
R3A1	ERJ3GEYJ473	47K		1
R3A2	ERJ3GEYJ473	47K		1
R3A3	ERJ3GEYJ473	47K		1
R3A4	ERJ3GEYJ473	47K		1
R3A5	ERJ3GEYJ473	47K		1
R3A6	ERJ3GEYJ473	47K		1
R3A7	ERJ3GEYJ473	47K		1
R3A8	ERJ3GEYJ473	47K		1
R3A9	ERJ3GEYJ473	47K		1

This replacement parts list is for KX-TVS200 only. Refer to the simplified manual (cover) for other areas.

Ref. No.	Part No.	Part Name & Description		Pcs
R3B0	PQ4R10XJ103	10K	S	1
R3B1	PQ4R10XJ103	10K	S	1
R3B2	PQ4R10XJ103	10K	S	1
R3B3	PQ4R10XJ103	10K	S	1
R3B4	PQ4R10XJ103	10K	S	1
R3B5	PQ4R10XJ103	10K	S	1
R3B6	PQ4R10XJ103	10K	S	1
R3B7	PQ4R10XJ103	10K	S	
R3C0	PQ4R10XJ472	4.7K	S	1
R3C1	PQ4R10XJ472	4.7K	S	1
R3C2	PQ4R10XJ472	4.7K	S	1
R3C3	PQ4R10XJ472	4.7K	S	1
R3D0	ERJ3GEYJ330	33		1
R3D1	ERJ3GEYJ330	33		1
R3D2	ERJ3GEYJ330	33		1
R3D3	ERJ3GEYJ330	33		1
R3D4	ERJ3GEYJ330	33		1
R3D5	ERJ3GEYJ330	33		1
R3D6	ERJ3GEYJ330	33		1
R3D7	ERJ3GEYJ330	33		1
R3D8	ERJ3GEYJ330	33		1
R3D9	ERJ3GEYJ330	33		1
R3E0	ERJ3GEYJ330	33		1
R3E1	ERJ3GEYJ330	33		1
R3E2	ERJ3GEYJ330	33		1
R3E3	ERJ3GEYJ330	33		1
R3E4	ERJ3GEYJ330	33		1
R3E5	ERJ3GEYJ330	33		1
R3E6	ERJ3GEYJ330	33		1
R3E7	ERJ3GEYJ330	33		1
R3E8	ERJ3GEYJ330	33		1
R3E9	ERJ3GEYJ330	33		1
R3F0	ERJ3GEYJ330	33		1
R3F1	ERJ3GEYJ330	33		1
R3F2	ERJ3GEYJ330	33		1
R3F3	ERJ3GEYJ101	100		1
R3F4	ERJ3GEYJ101	100		1
R3F5	ERJ3GEYJ330	33		1
R3F6	ERJ3GEYJ330	33		1
R3F7	ERJ3GEYJ101	100		1
R3F8	ERJ3GEYJ101	100		1
R3F9	ERJ3GEYJ101	100		1
R3G0	ERJ3GEYJ101	100		1
R3G1	ERJ3GEYJ101	100		1
R3G2	ERJ3GEYJ101	100		1
R3G3	ERJ3GEYJ101	100		1
R3G4	ERJ3GEYJ101	100		1
R3G5	ERJ3GEYJ101	100		1
R3G6	ERJ3GEYJ101	100		1
R3G7	ERJ3GEYJ101	100		1
R3G8	ERJ3GEYJ101	100		1
R3G9	ERJ3GEYJ101	100		
R3H0	ERJ3GEYJ101	100		1
R3H1	ERJ3GEYJ101	100		1
R3H2	ERJ3GEYJ101	100		1
R3H3	ERJ3GEYJ101	100		1
R3H4	ERJ3GEYJ101	100		1
R3H5	ERJ3GEYJ101	100		1
R3H6	ERJ3GEYJ103	10K		1
R3H7	ERJ3GEYJ103	10K		1
R3H8	ERJ3GEYJ103	10K		1
R3H9	ERJ3GEYJ103	10K		1

Ref. No.	Part No.	Part Name & Description		Pcs
R3J0	ERJ3GEYJ103	10K		1
R3J1	ERJ3GEYJ103	10K		1
R3J2	PQ4R10XJ103	10K	S	1
R3J3	PQ4R10XJ103	10K	S	1
R3J4	PQ4R10XJ103	10K	S	1
R3J5	PQ4R10XJ103	10K	S	1
R3J6	PQ4R10XJ103	10K	S	1
R3J7	PQ4R10XJ103	10K	S	1
R3J8	PQ4R10XJ103	10K	S	1
R3J9	ERJ3GEYJ103	10K		1
R3K0	ERJ3GEYJ103	10K		1
R3K1	ERJ3GEYJ103	10K		1
R3K2	ERJ3GEYJ103	10K		1
R3K3	ERJ3GEYJ103	10K		1
R3K4	ERJ3GEYJ103	10K		1
R3K5	ERJ3GEYJ103	10K		1
R3K6	ERJ3GEYJ103	10K		1
R3K7	ERJ3GEYJ103	10K		1
R3K8	ERJ3GEYJ103	10K		1
R3K9	ERJ3GEYJ103	10K		1
R3L0	ERJ3GEYJ103	10K		1
R3L1	ERJ3GEYJ103	10K		1
R3L2	ERJ3GEYJ103	10K		1
R3L3	ERJ3GEYJ103	10K		1
R3L4	ERJ3GEYJ103	10K		1
R3L5	PQ4R10XJ152	1.5K	S	1
R3L6	ERJ3GEY0R00	0		1
R3L9	ERJ3GEYJ330	33		1
R3M0	ERJ3GEYJ330	33		1
R3M1	ERJ3GEYJ330	33		1
R3N0	ERJ3GEYJ103	10K		1
R3N1	ERJ3GEYJ103	10K		1
R3N2	ERJ3GEYJ103	10K		1
R3N3	ERJ3GEYJ103	10K		1
R3N4	ERJ3GEYJ103	10K		1
R3N5	ERJ3GEYJ103	10K		1
R3N6	ERJ3GEYJ103	10K		1
R3N7	ERJ3GEYJ103	10K		1
R3N8	ERJ3GEYJ103	10K		1
R3N9	ERJ3GEYJ103	10K		1
R3P0	ERJ3GEY0R00	0		1
R3P1	ERJ3GEY0R00	0		1
R3P2	ERJ3GEY0R00	0		1
R3P3	ERJ3GEY0R00	0		1
R3P4	ERJ3GEY0R00	0		1
R3P5	ERJ3GEY0R00	0		1
R3P6	ERJ3GEY0R00	0		1
R3P7	ERJ3GEY0R00	0		1
R3P8	ERJ3GEY0R00	0		1
R3P9	ERJ3GEY0R00	0		1
R3S4	ERJ3GEYJ330	33		1
R3S5	ERJ3GEYJ330	33		1
R3S6	ERJ3GEYJ330	33		1
R3S7	ERJ3GEYJ330	33		1
R3S8	ERJ3GEYJ330	33		1
R3S9	ERJ3GEYJ330	33		1
R3T1	ERJ3GEYJ820	82		1
R3T2	ERJ3GEYJ820	82		1
R3T3	ERJ3GEYJ820	82		1
R3T5	ERJ3GEYJ330	33		1
R3T6	ERJ3GEYJ330	33		1
R3T7	ERJ3GEYJ330	33		1
R3T8	ERJ3GEYJ330	33		1
R3T9	ERJ3GEYJ330	33		1

This replacement parts list is for KX-TVS200 only. Refer to the simplified manual (cover) for other areas.

Ref. No.	Part No.	Part Name & Description		Pcs
R3U0	ERJ3GEYJ330	33		1
R3U2	ERJ3GEYJ330	33		1
R3U3	ERJ3GEY0R00	0		1
R3U6	ERJ3GEYJ330	33		1
R3U7	ERJ3GEYJ330	33		1
R3U8	ERJ3GEYJ330	33		1
R3U9	ERJ3GEY0R00	0		1
R3W1	ERJ3GEYJ330	33		1
R3W2	ERJ3GEYJ473	47K		1
R3W3	ERJ3GEYJ101	100		1
R3W5	ERJ3GEYJ330	33		1
R3W6	ERJ3GEYJ330	33		1
R3W7	ERJ3GEYJ330	33		1
R3W9	ERJ3GEY0R00	0		1
R3X0	ERJ3GEY0R00	0		1
R3X1	ERJ3GEY0R00	0		1
R3X2	ERJ3GEY0R00	0		1
R3X3	ERJ3GEY0R00	0		1
R3X4	ERJ3GEY0R00	0		1
R3X5	ERJ3GEY0R00	0		1
R3X6	ERJ3GEY0R00	0		1
R3X7	ERJ3GEY0R00	0		1
R3Y1	ERJ3GEYJ472	4.7K		1
R301,302	ERJ3GEYJ330	33		2
R303	PQ4R10XJ472	4.7K	S	1
R304,305	ERJ3GEYJ472	4.7K		2
R306	ERJ3GEYJ103	10K		1
R307	ERJ3GEYJ472	4.7K		1
R308	ERJ3GEYJ472	4.7K		1
R309	ERJ3GEYJ472	4.7K		1
R310	ERJ3GEYJ101	100		1
R311	ERJ3GEY0R00	0		1
R312	ERJ3GEYJ101	100		1
R313-319	ERJ3GEYJ330	33		7
R320	PQ4R10XJ472	4.7K	S	1
R321	ERJ3GEY0R00	0		1
R323	ERJ3GEYJ470	47		1
R324	ERJ3GEYJ330	33		1
R326	ERJ3GEYJ560	56		1
R327	PQ4R10XJ821	820	S	1
R329	PQ4R10XJ820	82	S	1
R330	ERJ3GEYJ221	220		1
R331,332	ERJ3GEYJ473	47K		2
R333	PQ4R10XJ473	47K		1
R334	ERJ3GEYJ472	4.7K		1
R336-339	PQ4R10XJ473	47K	S	4
R340,341	ERJ3GEY0R00	0		2
R342	ERJ3GEYJ103	10K		1
R343-349	ERJ3GEY0R00	0		7
R350-359	ERJ3GEY0R00	0		10
R360	ERJ3GEYJ184	180K		1
R362	ERJ3GEYJ330	33		1
R363-369	ERJ3GEYJ101	100		7
R370	PQ4R10XJ103	10K	S	1
R372	PQ4R10XJ473	47K	S	1
R373,374	ERJ3GEYJ473	47K		2
R375	PQ4R10XJ473	47K	S	1
R376	PQ4R10XJ103	10K	S	1
R377	ERJ3GEY0R00	0		1
R378	ERJ3GEY0R00	0		1
R379	ERJ3GEY0R00	0		1
R380-389	ERJ3GEY0R00	0		10
R390-399	ERJ3GEY0R00	0		10
R801	PQ4R10XJ221	220	S	1
		(COILS)		
R3Q0	PQLQR1RM601	COIL		1
R3Q1	PQLQR1RM601	COIL		1
R3Q2	PQLQR1RM601	COIL		1
R3Q3	PQLQR1RM601	COIL		1
R3Q4	PQLQR1RM601	COIL		1
R3Q5	PQLQR1RM601	COIL		1
R3Q6	PQLQR1RM601	COIL		1
R3Q7	PQLQR1RM601	COIL		1
R3Q8	PQLQR1RM601	COIL		1
R3Q9	PQLQR1RM601	COIL		1
R3R0	PQLQR1RM601	COIL		1
R3R1	PQLQR1RM601	COIL		1
R3R2	PQLQR1RM601	COIL		1
R3R3	PQLQR1RM601	COIL		1
R3R4	PQLQR1RM601	COIL		1
R3R5	PQLQR1RM601	COIL		1
R3V4	PQLQR1RM601	COIL		1
R3W0	PQLQR1RM601	COIL		1
R3X8	PQLQR1RM601	COIL		1
R3X9	PQLQR1RM601	COIL		1
R325	PQLQR1RS121	COIL		1
		(SWITCH)		
SW301	PQSR10A101Z	ROTARY SWITCH		1
		(CRYSTAL OSCILLATORS)		
X300	PQVCL3276N6Z	CRYSTAL OSCILLATOR		1
X301	PSVCCR3276B2	CRYSTAL OSCILLATOR	S	1

FIXTURES AND TOOLS

EC1	PSZZ40K3Z	EXTENSION CORD, 40P	1
EC2	PSZZ4K9Z	EXTENSION CORD, 4P	1
EC3	PQZZ50K4Z	EXTENSION CORD, 50P	1

Notes:
Extension cords are useful for servicing.
(They make servicing easy.)

This replacement parts list is for KX-TVS204 only. Refer to the simplified manual (cover) for other areas.

REPLACEMENT PARTS LIST
Model KX-TVS204

Notes:

1. The marking (RTL) indicates that the Retention Time is limited for this item. After the discontinuation of this assembly in production, the item will continue to be available for a specific period of time. The retention period of availability is dependent on the type of assembly, and in accordance with the laws governing part and product retention. After the end of this period, the assembly will no longer be available.
2. Important safety notice.
   Components identified by the mark special characteristics important for safety.
   When replacing any of these components, use only manufacturer's specified parts.
3. The S mark indicates service standard parts and may differ from production parts.
4. RESISTORS & CAPACITORS
   Unless otherwise specified.
   All resistors are in ohms (Ω) k=1000Ω, M=1000kΩ
   All capacitors are in MICRO FARADS(μF) P= μμF
   *Type &Wattage of Resistor
   Type

ERC:Solid	ERX:Metal Film	PQRD:Carbon
ERD:Carbon	ERG:Metal Oxide	PQRQ:Fuse
PQ4R:Chip	ERO:Metal Film	ERF:Wire Wound

Wattage

10,16,18:1/8W	14,25,S2:1/4W	12,50,S1:1/2W	1:1W	2:2W	5:5W

*Type & Voltage of Capacitor
Type

ECFD:Semi-Conductor	ECCD,ECKD,PQCBC,PQVP : Ceramic
ECQS:Styrol	ECQM,ECQV,ECQE,ECQU,ECQB : Polyester
PQCBX,ECUV:Chip	ECEA,ECSZ,ECOS : Electrolytic
ECMS:Mica	ECQP : Polypropylene

Voltage

ECQ Type	ECQG ECQV Type	ECSZ Type	Others	
1H: 50V	05: 50V	OF:3.15V	OJ :6.3V	1V :35V
2A:100V	1:100V	1A:10V	1A :10V	50,1H:50V
2E:250V	2:200V	1V:35V	1C :16V	1J :63V
2H:500V		OJ:6.3V	1E,25:25V	2A :100V

Ref. No.	Part No.	Part Name & Description		Pcs
		BOARD PARTS		
		(ICs)		
IC101A	PQVIPD656214	IC		1
IC101B	PQVIPD656214	IC		1
IC102	PQVISN7L244S	IC	S	1
IC103	PQVISN7L244S	IC	S	1
IC104	PQVISN7L245S	IC	S	1
IC105	PQVISN7L241M	IC	S	1
IC106A	PQVISN7L126A	IC	S	1
IC106B	PQVISN7L126A	IC	S	1
IC107	PSVITC7S08FU	IC		1
IC108	PSVITC7S32FU	IC		1
IC109A	PSVI8C060BPJ	IC		1
IC109B	PSVI8C060BPJ	IC		1
IC109C	PSVI8C060BPJ	IC		1
IC109D	PSVI8C060BPJ	IC		1
IC261A	PQVINJM319V	IC		1
IC261B	PQVINJM319V	IC		1
		(TRANSISTORS)		
Q100A	PQVTDTC143E	TRANSISTOR(SI)		1
Q100B	PQVTDTC143E	TRANSISTOR(SI)		1
Q261A	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	S	1
Q261B	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	S	1
Q262A	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	S	1
Q262B	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	S	1
		(CONNECTORS & JACK)		
CN101	PQJP50S33Z	CONNECTOR, 50P		1
CN102	PSJP60A45Z	CONNECTOR, 60P		1
CN103	PSJJ2T004Z	JACK, TEL		1
		(CAPACITORS)		
C100	ECUV1H102KBV	0.001		1
C101A	ECUV1H102KBV	0.001		1
C101B	ECUV1H102KBV	0.001		1
C102A	ECUV1H120JCV	12P		1
C102B	ECUV1H120JCV	12P		1
C103A	ECUV1H120JCV	12P		1
C103B	ECUV1H120JCV	12P		1
C104A	ECUV1C104KBV	0.1	S	1
C104B	ECUV1C104KBV	0.1	S	1
C105A	ECUV1C104KBV	0.1	S	1
C105B	ECUV1C104KBV	0.1	S	1
C106A	ECUV1H101JCV	100P		1
C106B	ECUV1H101JCV	100P		1
C107A	ECUV1H101JCV	100P		1
C107B	ECUV1H101JCV	100P		1
C108A	ECUV1H102KBV	0.001		1
C108B	ECUV1H102KBV	0.001		1
C109A	ECUV1H102KBV	0.001		1
C109B	ECUV1H102KBV	0.001		1
C110A	ECUV1H102KBV	0.001		1
C110B	ECUV1H102KBV	0.001		1
C111A	ECUV1H102KBV	0.001		1
C111B	ECUV1H102KBV	0.001		1
C112A	ECUV1H102KBV	0.001		1
C112B	ECUV1H102KBV	0.001		1
C113A	ECUV1H102KBV	0.001		1
C113B	ECUV1H102KBV	0.001		1
C114A	ECUV1H102KBV	0.001		1
C114B	ECUV1H102KBV	0.001		1
C114C	ECUV1H102KBV	0.001		1
C114D	ECUV1H102KBV	0.001		1
C115A	ECUV1C104KBV	0.1	S	1
C115B	ECUV1C104KBV	0.1	S	1
C115C	ECUV1C104KBV	0.1	S	1
C115D	ECUV1C104KBV	0.1	S	1
C116A	PQCUV1H223KB	0.022		1
C116B	PQCUV1H223KB	0.022		1
C116C	PQCUV1H223KB	0.022		1
C116D	PQCUV1H223KB	0.022		1
C117A	ECUV1C391JCV	390P		1
C117B	ECUV1C391JCV	390P		1
C117C	ECUV1C391JCV	390P		1
C117D	ECUV1C391JCV	390P		1
C118A	ECUV1C104KBV	0.1	S	1
C118B	ECUV1C104KBV	0.1	S	1
C118C	ECUV1C104KBV	0.1	S	1
C118D	ECUV1C104KBV	0.1	S	1
C119A	PQCUV1H105JC	1	S	1
C119B	PQCUV1H105JC	1	S	1
C119C	PQCUV1H105JC	1	S	1
C119D	PQCUV1H105JC	1	S	1

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Ref. No.	Part No.	Part Name & Description		Pcs
C120A	ECUV1C104KBV	0.1	S	1
C120B	ECUV1C104KBV	0.1	S	1
C120C	ECUV1C104KBV	0.1	S	1
C120D	ECUV1C104KBV	0.1	S	1
C121A	ECUV1C104KBV	0.1	S	1
C121B	ECUV1C104KBV	0.1	S	1
C121C	ECUV1C104KBV	0.1	S	1
C121D	ECUV1C104KBV	0.1	S	1
C122E	ECUV1H220JCV	22P		1
C123E	ECUV1H100DCV	10P	S	1
C130	ECEA1AU221	220		1
C131-139	ECUV1C104KBV	0.1	S	1
C140-147	ECUV1C104KBV	0.1	S	1
C230A	ECUV1C104KBV	0.1	S	1
C230B	ECUV1C104KBV	0.1	S	1
C233A	ECUV1C104KBV	0.1	S	1
C233B	ECUV1C104KBV	0.1	S	1
C234A	ECUV1C104KBV	0.1	S	1
C234B	ECUV1C104KBV	0.1	S	1
C261A	ECEV1HA010	1		1
C261B	ECEV1HA010	1		1
C262A	ECEV1HA010	1		1
C262B	ECEV1HA010	1		1
C263A	ECUV1H680JCV	68P		1
C263B	ECUV1H680JCV	68P		1
C264A	ECUV1H680JCV	68P		1
C264B	ECUV1H680JCV	68P		1
C265A	ECUV1H101JCV	100P		1
C265B	ECUV1H101JCV	100P		1
C266A	ECUV1H101JCV	100P		1
C266B	ECUV1H101JCV	100P		1
C267A	ECUV1H470JCV	47P		1
C267B	ECUV1H470JCV	47P		1
C268A	ECUV1H470JCV	47P		1
C268B	ECUV1H470JCV	47P		1
C269A	PQCUV1H223KB	0.022		1
C272A	ECUV1C104KBV	0.1	S	1
C272B	ECUV1C104KBV	0.1	S	1
C291A	ECEA1HN2R2S	2.2	S	1
C291B	ECEA1HN2R2S	2.2	S	1
		(COILS)		
L110	PQLQR1RS121	COIL		1
L112A	PQLQR1RS121	COIL		1
L112B	PQLQR1RS121	COIL		1
L291A	PQLQR1LT	COIL		1
L291B	PQLQR1LT	COIL		1
L292A	PQLQR1LT	COIL		1
L292B	PQLQR1LT	COIL		1

Ref. No.	Part No.	Part Name & Description	Pcs
		(RESISTORS)	
L111	ERJ3GEY0R00	0	1
R100A	ERJ3GEYJ330	33	1
R100B	ERJ3GEYJ330	33	1
R102	ERJ3GEYJ330	33	1
R105A	ERJ3GEYJ473	47K	1
R105B	ERJ3GEYJ473	47K	1
R107A	ERJ3GEY0R00	0	1
R107B	ERJ3GEY0R00	0	1
R108A	ERJ3GEYJ471	470	1
R108B	ERJ3GEYJ471	470	1
R110A	ERJ3GEYJ330	33	1
R110B	ERJ3GEYJ330	33	1
R111A	ERJ3GEYJ330	33	1
R111B	ERJ3GEYJ330	33	1
R112A	ERJ3GEYJ330	33	1
R112B	ERJ3GEYJ330	33	1
R113A	ERJ3GEYJ330	33	1
R113B	ERJ3GEYJ330	33	1
R114A	ERJ3GEYJ330	33	1
R114B	ERJ3GEYJ330	33	1
R115A	ERJ3GEYJ473	47K	1
R115B	ERJ3GEYJ473	47K	1
R115C	ERJ3GEYJ473	47K	1
R115D	ERJ3GEYJ473	47K	1
R116A	ERJ3GEYJ272	2.7K	1
R116B	ERJ3GEYJ272	2.7K	1
R116C	ERJ3GEYJ272	2.7K	1
R116D	ERJ3GEYJ272	2.7K	1
R117A	ERJ3GEYJ473	47K	1
R117B	ERJ3GEYJ473	47K	1
R117C	ERJ3GEYJ473	47K	1
R117D	ERJ3GEYJ473	47K	1
R118A	ERJ3GEYJ473	47K	1
R118B	ERJ3GEYJ473	47K	1
R118C	ERJ3GEYJ473	47K	1
R118D	ERJ3GEYJ473	47K	1
R119A	ERJ3GEYJ473	47K	1
R119B	ERJ3GEYJ473	47K	1
R119C	ERJ3GEYJ473	47K	1
R119D	ERJ3GEYJ473	47K	1
R120A	ERJ3GEYJ473	47K	1
R120B	ERJ3GEYJ473	47K	1
R120C	ERJ3GEYJ473	47K	1
R120D	ERJ3GEYJ473	47K	1
R121A	ERJ3GEYJ473	47K	1
R121B	ERJ3GEYJ473	47K	1
R121C	ERJ3GEYJ473	47K	1
R121D	ERJ3GEYJ473	47K	1
R122A	ERJ3GEYJ473	47K	1
R122B	ERJ3GEYJ473	47K	1
R122C	ERJ3GEYJ473	47K	1
R122D	ERJ3GEYJ473	47K	1
R123A	ERJ3GEYJ473	47K	1
R123B	ERJ3GEYJ473	47K	1
R123C	ERJ3GEYJ473	47K	1
R123D	ERJ3GEYJ473	47K	1
R124A	ERJ3GEYJ473	47K	1
R124B	ERJ3GEYJ473	47K	1
R124C	ERJ3GEYJ473	47K	1
R124D	ERJ3GEYJ473	47K	1
R133	ERJ3GEYJ103	10K	1
R134	ERJ3GEYJ103	10K	1
R135	ERJ3GEYJ103	10K	1
R136	ERJ3GEYJ103	10K	1
R137 ✓	ERJ3GEYJ680	68	1
R138 ✓	ERJ3GEYJ470	47	1

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Ref. No.	Part No.	Part Name & Description	Pcs
R141A	ERJ3GEYJ473	47K	1
R141B	ERJ3GEYJ473	47K	1
R142A	ERJ3GEYJ473	47K	1
R142B	ERJ3GEYJ473	47K	1
R142C	ERJ3GEYJ473	47K	1
R142D	ERJ3GEYJ473	47K	1
R143A	ERJ3GEYJ103	10K	1
R143B	ERJ3GEYJ103	10K	1
R144A	ERJ3GEYJ103	10K	1
R144B	ERJ3GEYJ103	10K	1
R145A	ERJ3GEYJ103	10K	1
R145B	ERJ3GEYJ103	10K	1
R146A	ERJ3GEYJ103	10K	1
R146B	ERJ3GEYJ103	10K	1
R147A	ERJ3GEYJ103	10K	1
R147B	ERJ3GEYJ103	10K	1
R148A	ERJ3GEYJ103	10K	1
R148B	ERJ3GEYJ103	10K	1
R149A	ERJ3GEYJ103	10K	1
R149B	ERJ3GEYJ103	10K	1
R150B	ERJ3GEYJ103	10K	1
R261A	ERJ3GEYJ330	33	1
R261B	ERJ3GEYJ330	33	1
R262A	ERJ3GEYJ330	33	1
R262B	ERJ3GEYJ330	33	1
R263A	ERJ3GEYJ472	4.7K	1
R263B	ERJ3GEYJ472	4.7K	1
R264A	ERJ3GEYJ472	4.7K	1
R264B	ERJ3GEYJ472	4.7K	1
R265A	ERJ3GEYJ472	4.7K	1
R265B	ERJ3GEYJ472	4.7K	1
R266A	ERJ3GEYJ472	4.7K	1
R266B	ERJ3GEYJ472	4.7K	1
R267A	ERJ3GEYJ472	4.7K	1
R267B	ERJ3GEYJ472	4.7K	1
R268A	ERJ3GEYJ472	4.7K	1
R268B	ERJ3GEYJ472	4.7K	1
R269A	ERJ3GEYJ472	4.7K	1
R269B	ERJ3GEYJ472	4.7K	1
R270A	ERJ3GEYJ472	4.7K	1
R270B	ERJ3GEYJ472	4.7K	1
R271A	ERJ3GEYJ472	4.7K	1
R271B	ERJ3GEYJ472	4.7K	1
R272A	ERJ3GEYJ472	4.7K	1
R272B	ERJ3GEYJ472	4.7K	1
R273A	ERJ3GEYJ821	820	1
R273B	ERJ3GEYJ821	820	1
R274A	PQ4R10XF8201	8.2K	1
R275A	PQ4R10XF1201	1.2K	1
R276A	ERJ3GEYJ330	33	1
R276B	ERJ3GEYJ330	33	1
R277A	ERJ3GEYJ330	33	1
R277B	ERJ3GEYJ330	33	1
R291A	PQRQ1VJ821	820	1
R291B	PQRQ1VJ821	820	1

Ref. No.	Part No.	Part Name & Description	Pcs
		(TRANSFORMERS)	
T291A	PSLT9Z7A	TRANSFORMER	1
T291B	PSLT9Z7A	TRANSFORMER	1
		(CRYSTAL OSCILLATORS)	
X100A	PSVCCS1638G5	CRYSTAL OSCILLATOR	1
X100B	PSVCCS1638G5	CRYSTAL OSCILLATOR	1
		(VARISTORS)	
ZR291A	PSVDVF07820	VARISTOR	1
ZR291B	PSVDVF07820	VARISTOR	1
ZR292A	PSVDVF07820	VARISTOR	1
ZR292B	PSVDVF07820	VARISTOR	1
		(OTHERS)	
E1	PQDF996Z	SHAFT	2
E2	PSHR1104Z	GUIDE	2